

FIG.1

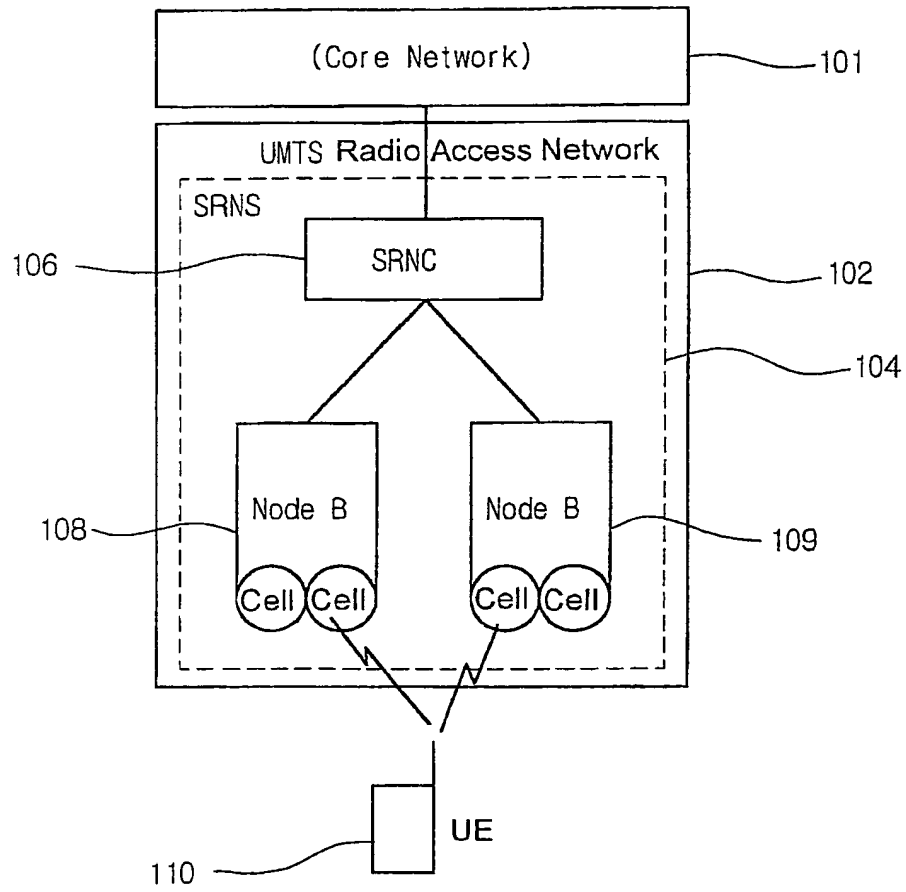


FIG.2

FIG. 2

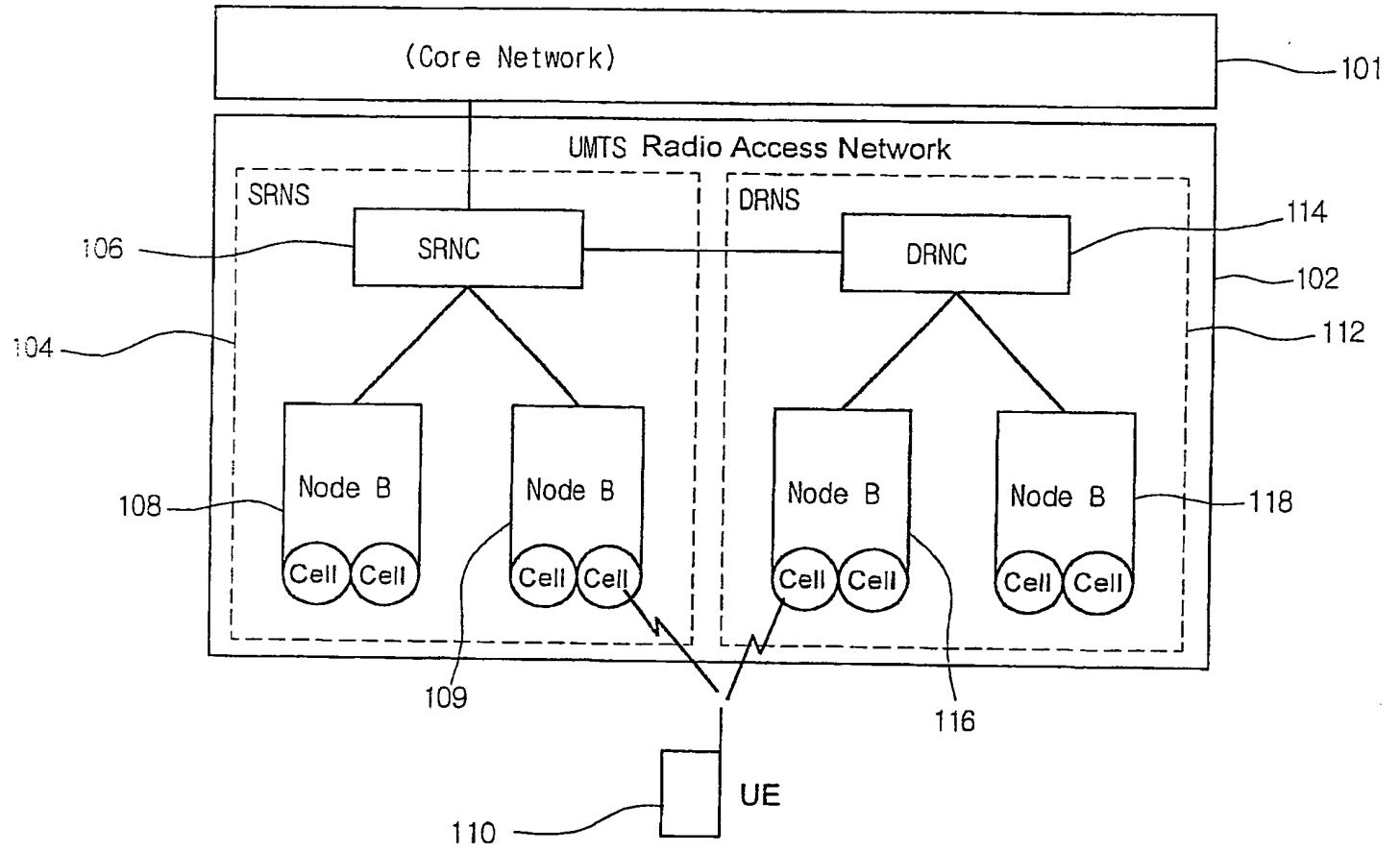


FIG.3

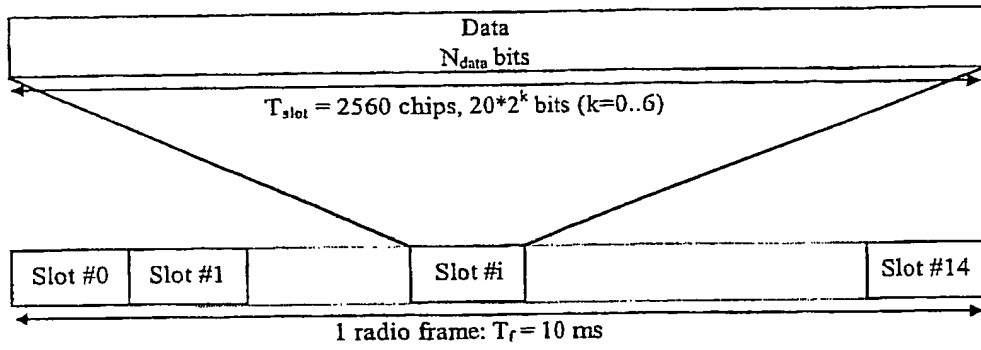


FIG.4

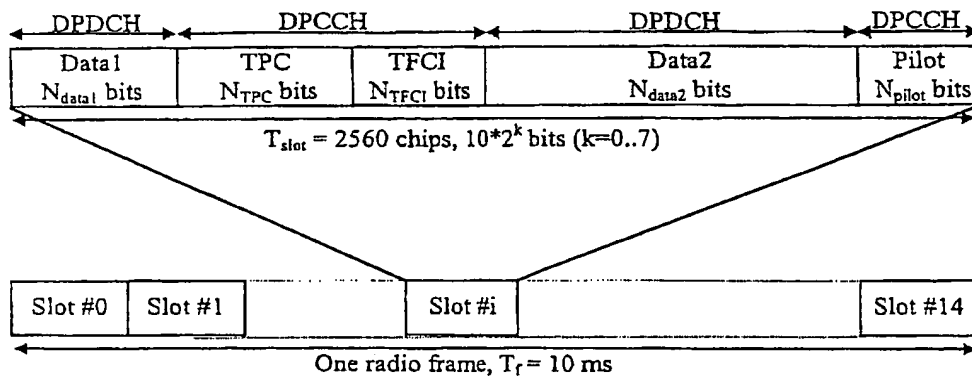


FIG.5

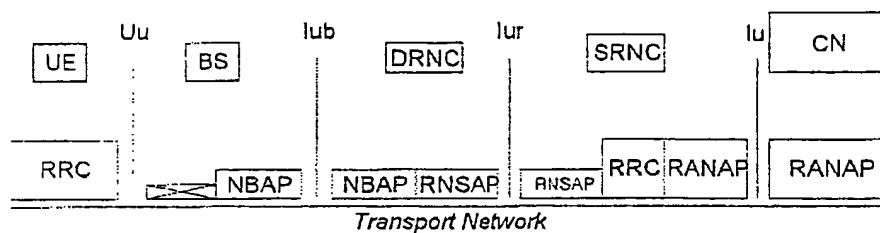


FIG.6

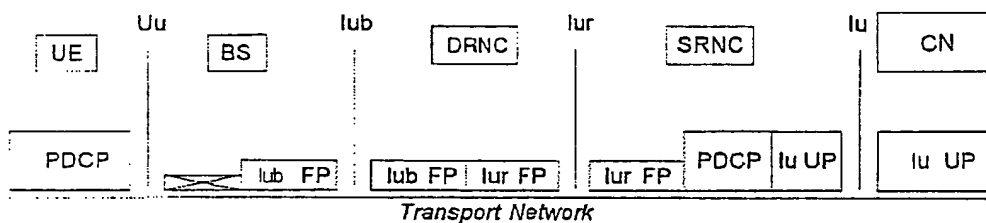


FIG.7

Control frame class	Coding
Outer loop power control	0000 0001
timing adjustment	0000 0010
DL synchronization	0000 0011
UL synchronization	0000 0100
DL signalling for DSCH	0000 0101
DL Node synchronization	0000 0110
UL Node synchronization	0000 0111
Rx Timing Deviation	0000 1000
Radio Interface Parameter Update	0000 1001
Timing Advance	0000 1010

FIG.8

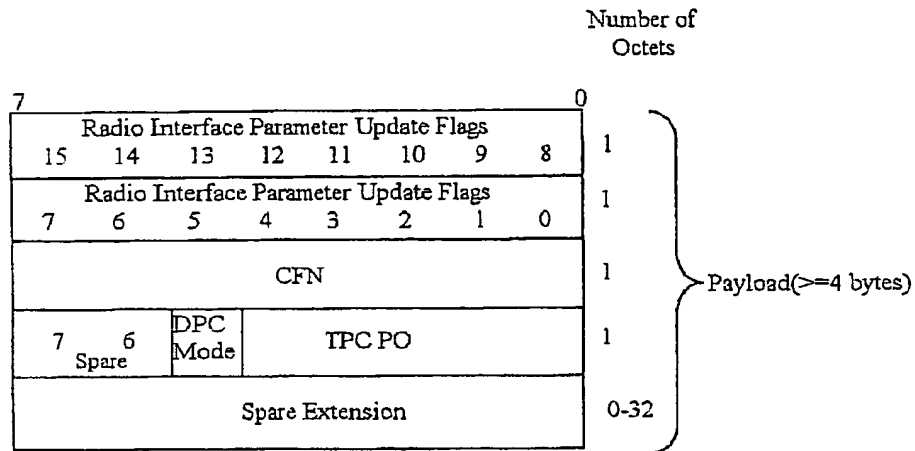
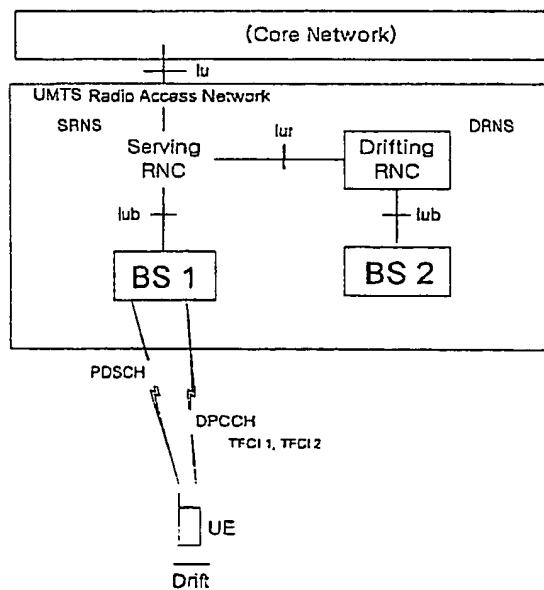


FIG.9A



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FIG.9B

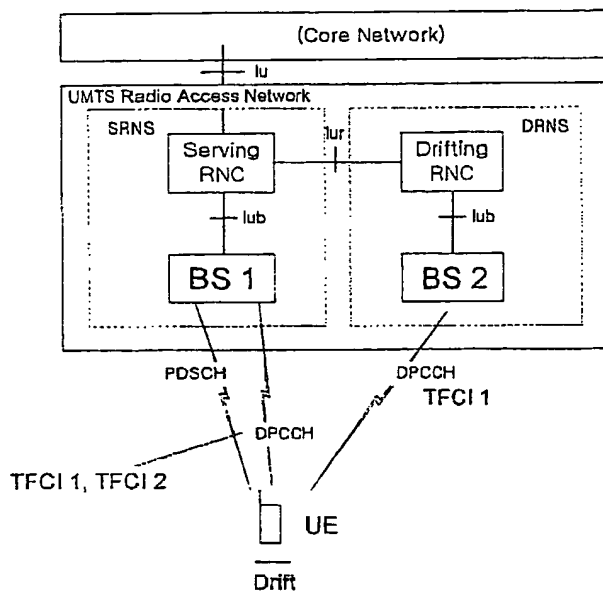


FIG.9C

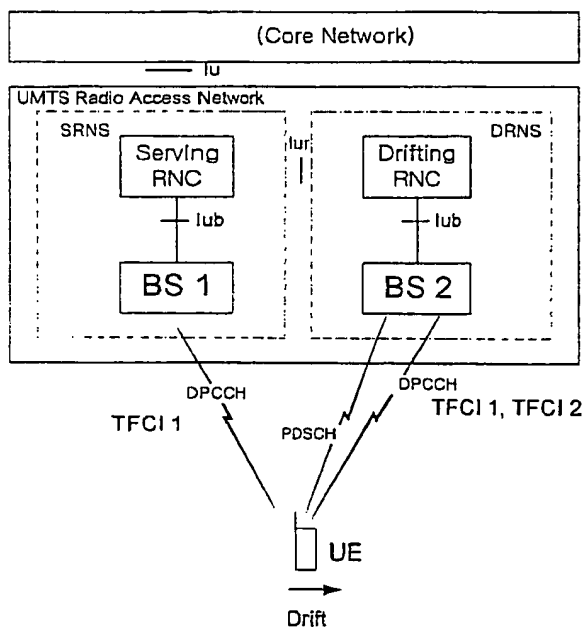


FIG.9D

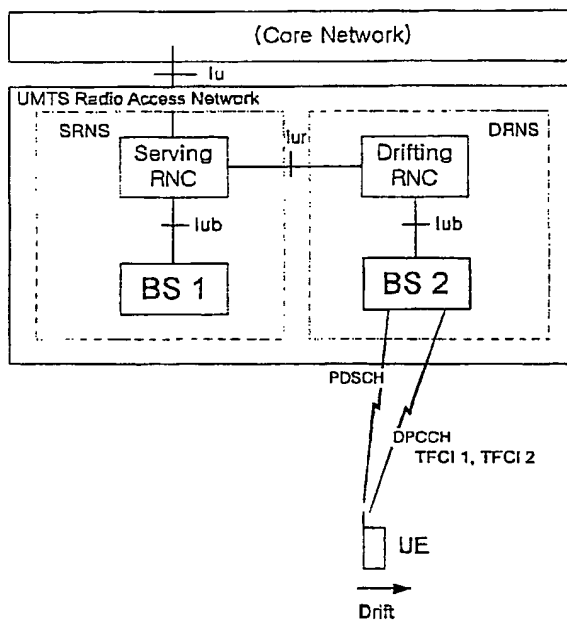


FIG.10A

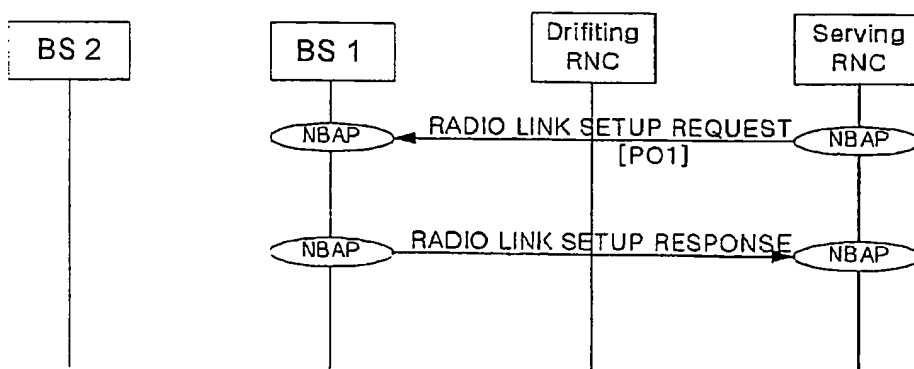


FIG.10B

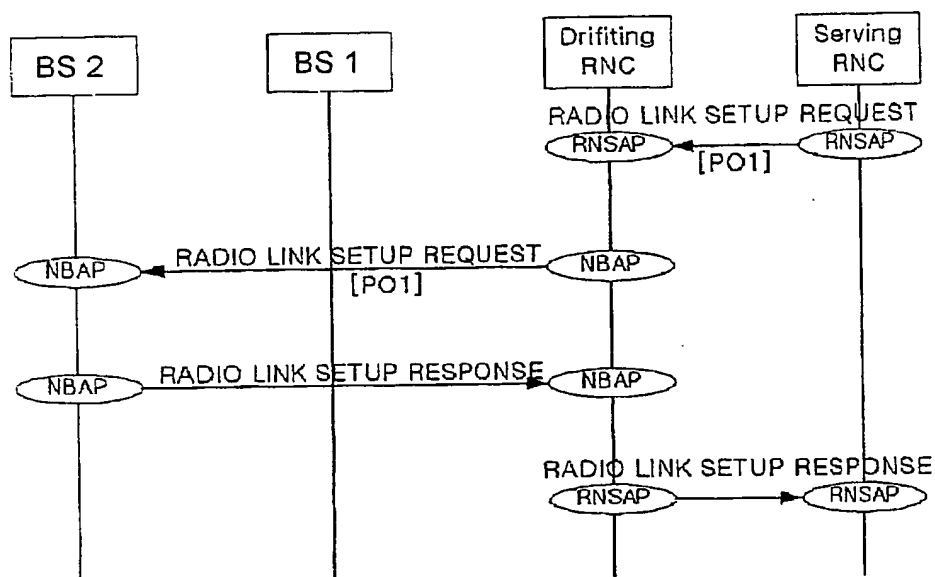


FIG.11

Slot Format #1	Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot			Transmitted slots per radio frame N_{Tr}
					N_{Data1}	N_{Data2}	N_{TPC}	N_{TFCI}	N_{Pilot}	
0	15	7.5	512	10	0	4	2	0	4	15
1	15	7.5	512	10	0	2	2	2	4	15
2	30	15	256	20	2	14	2	0	2	15
3	30	15	256	20	2	12	2	2	2	15
4	30	15	256	20	2	12	2	0	4	15
5	30	15	256	20	2	10	2	2	4	15
6	30	15	256	20	2	8	2	0	8	15
7	30	15	256	20	2	6	2	2	8	15
8	60	30	128	40	6	28	2	0	4	15
9	60	30	128	40	6	26	2	2	4	15
10	60	30	128	40	6	24	2	0	8	15
11	60	30	128	40	6	22	2	2	8	15
12	120	60	64	80	12	48	4	8*	8	15
13	240	120	32	160	28	112	4	8*	8	15
14	480	240	16	320	56	232	8	8*	16	15
15	960	480	8	640	120	488	8	8*	16	15
16	1920	960	4	1280	248	1000	8	8*	16	15

FIG.12

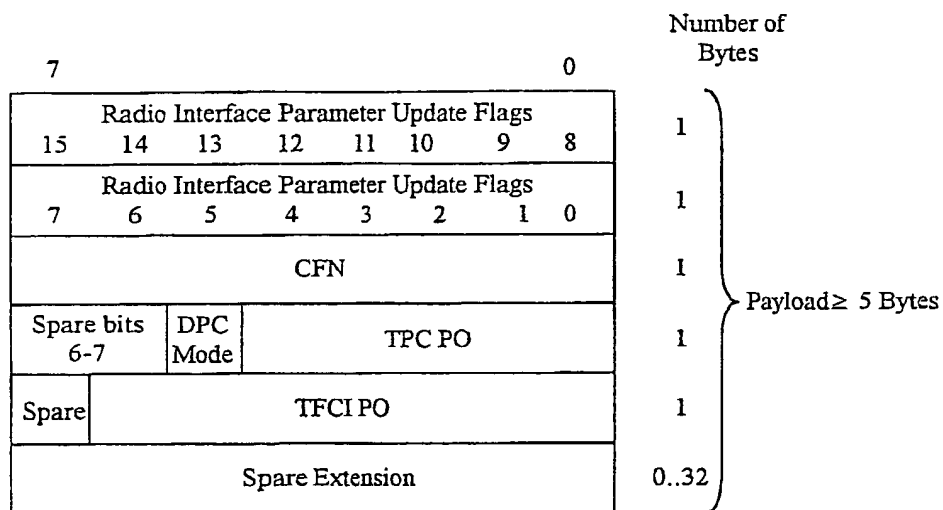


FIG.13

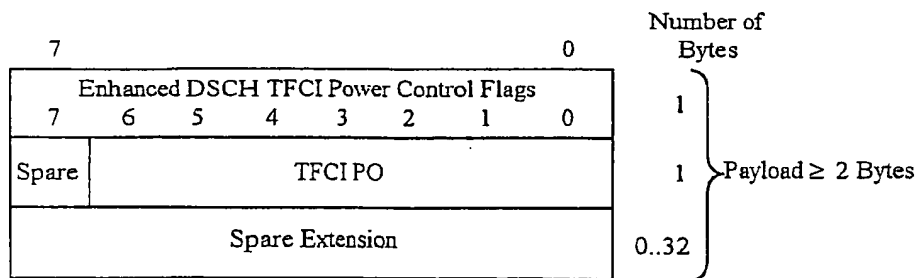


FIG.14A

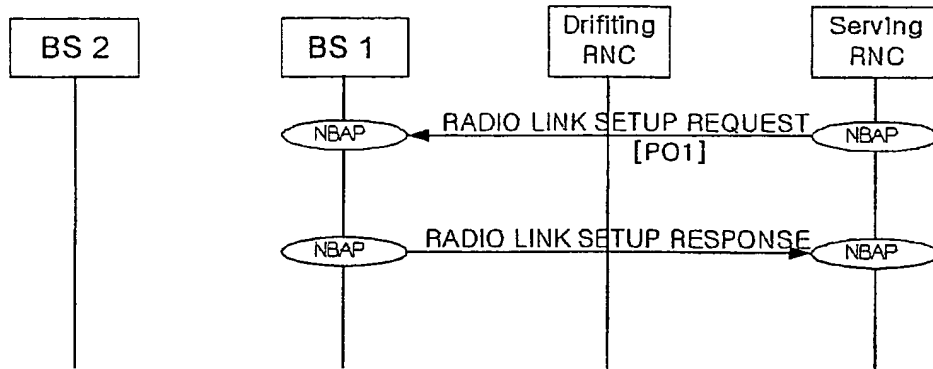


FIG.14B

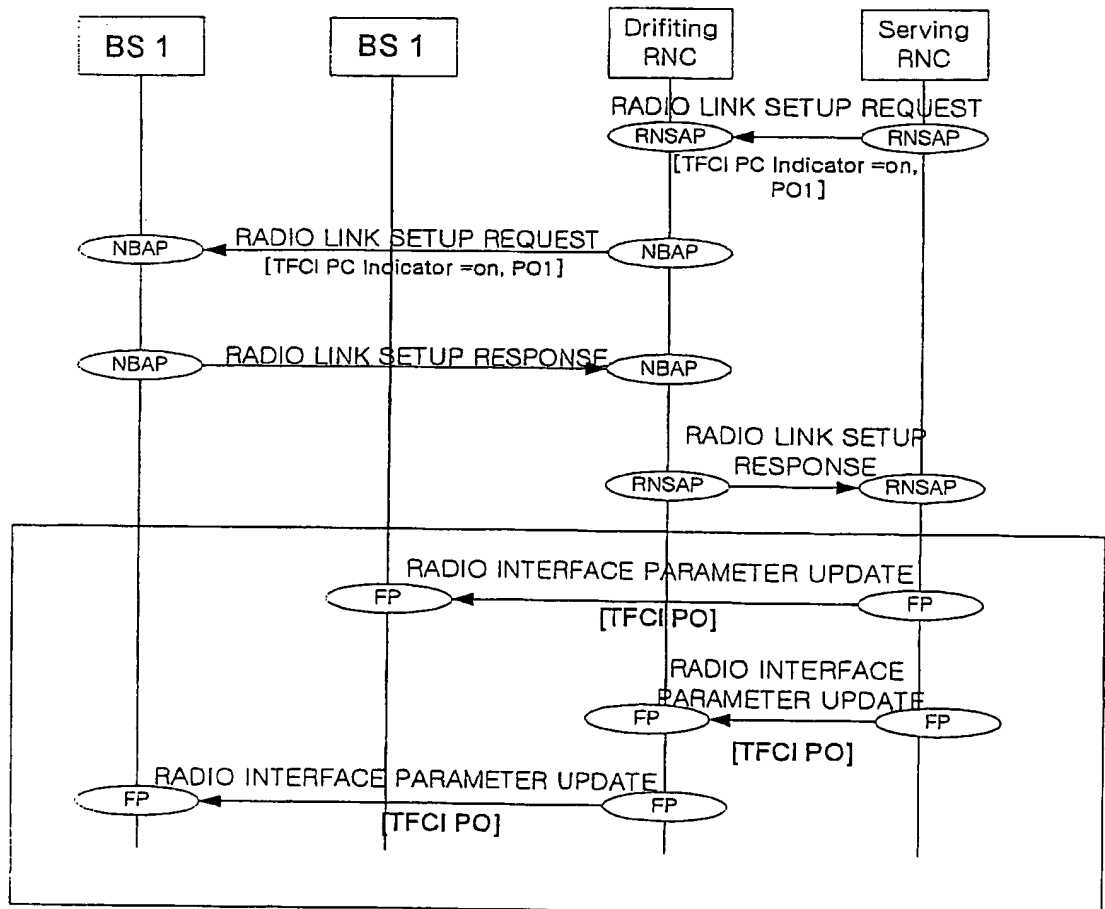


FIG.14C

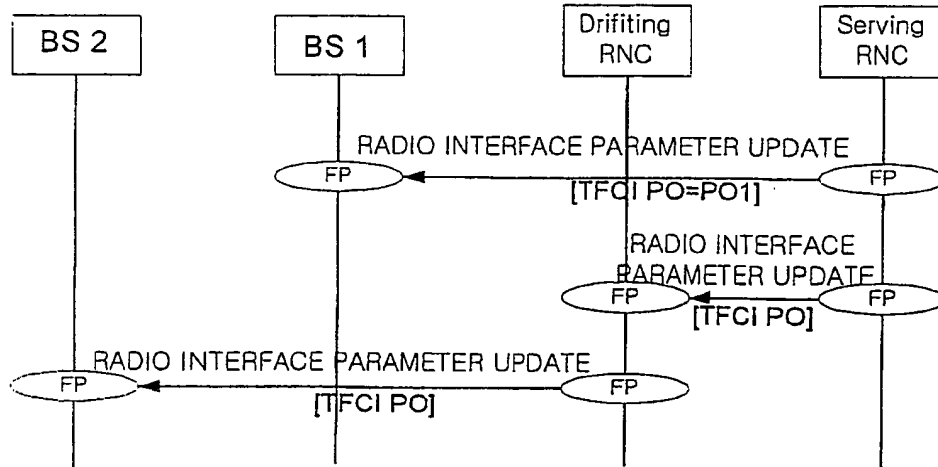


FIG.14D

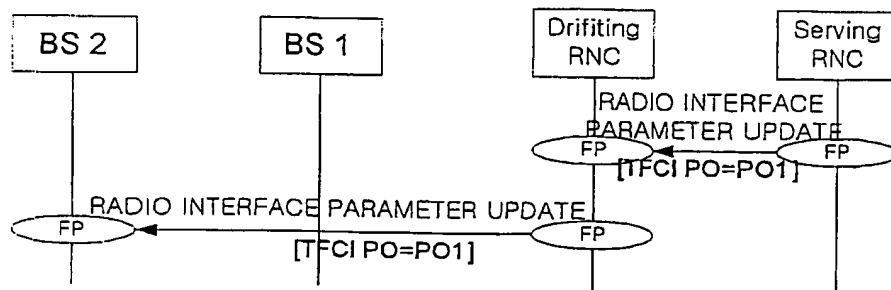


FIG.15A

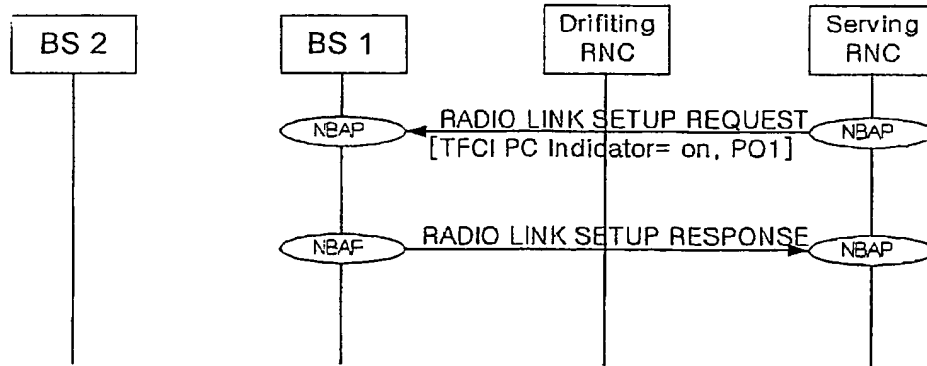


FIG.15B

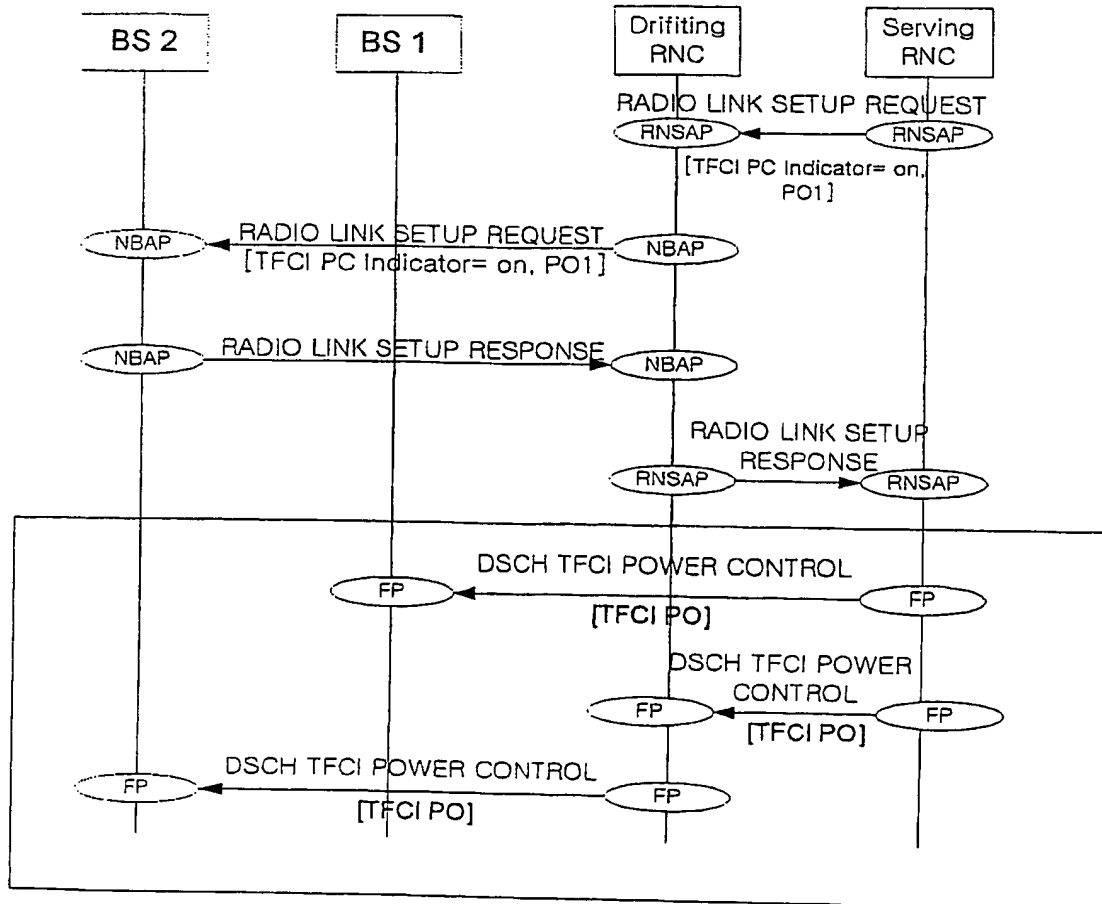


FIG.15C

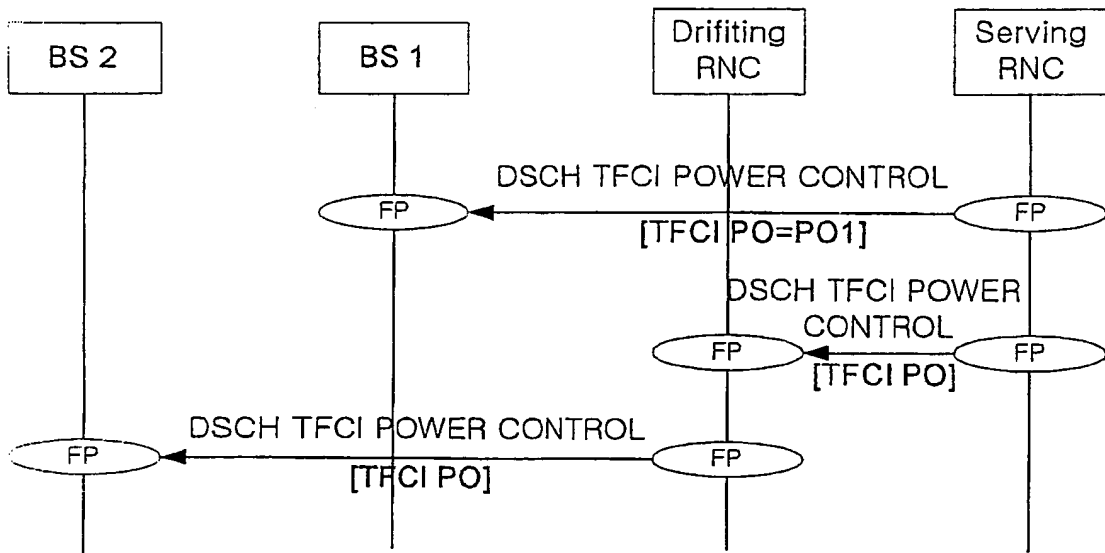


FIG.15D

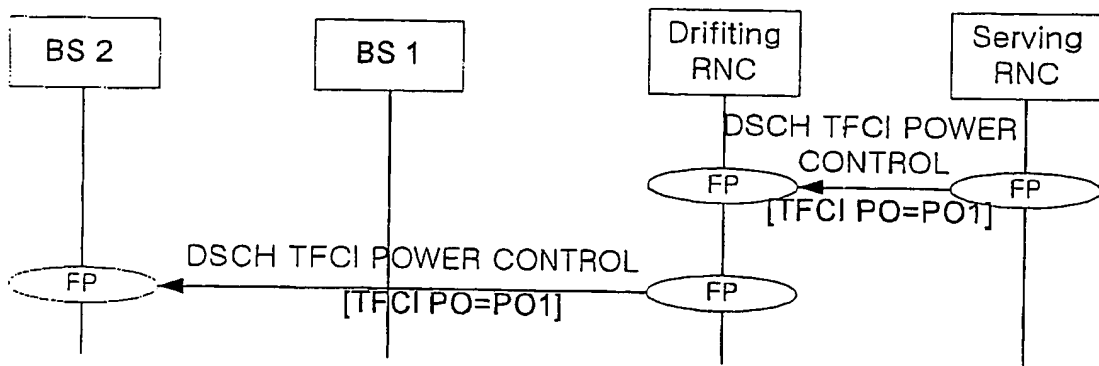
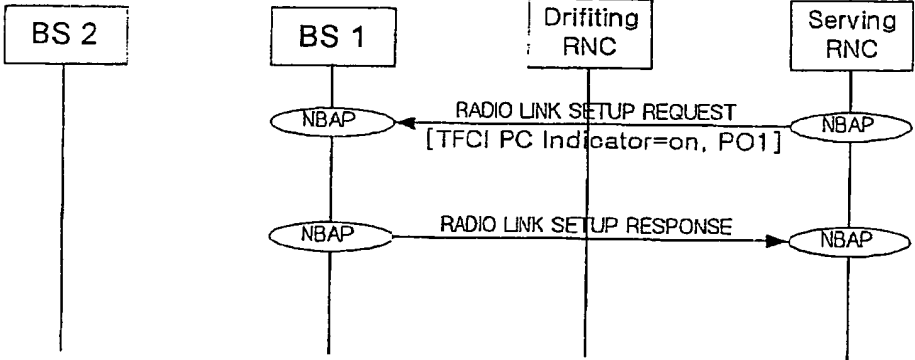


FIG.16A



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FIG.16B

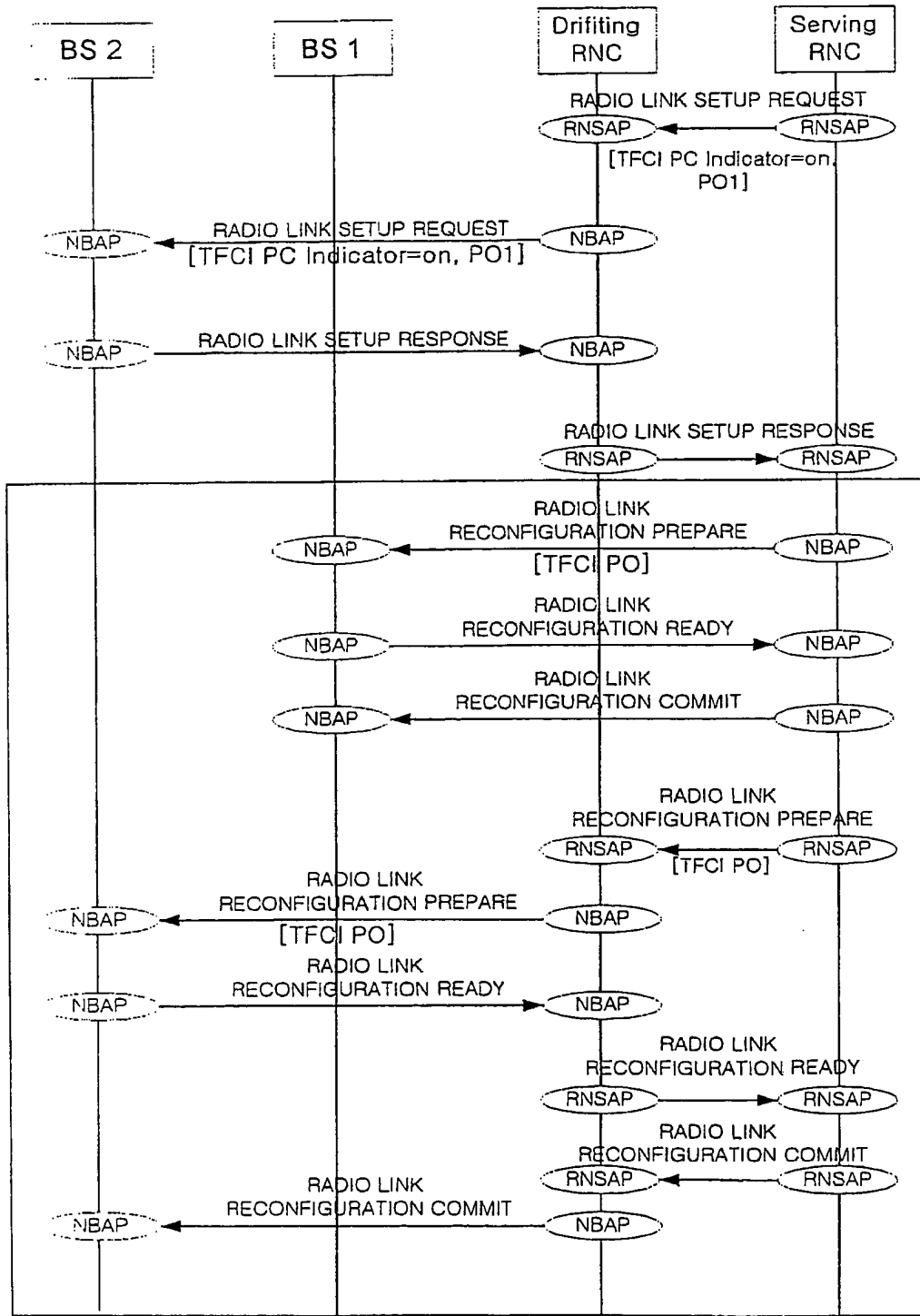


FIG. 16B

FIG.16C

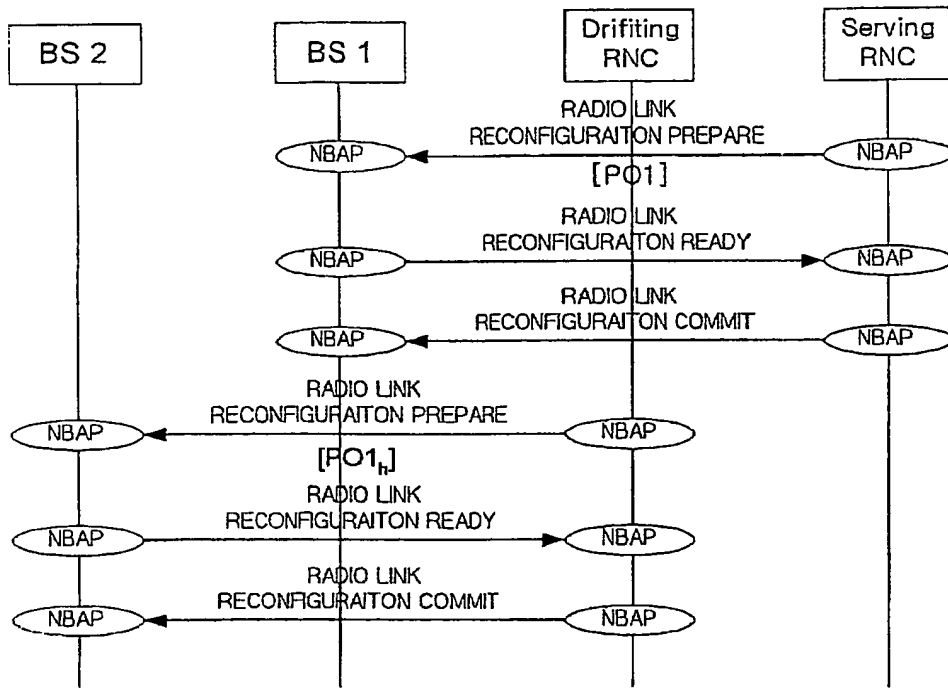


FIG.16D

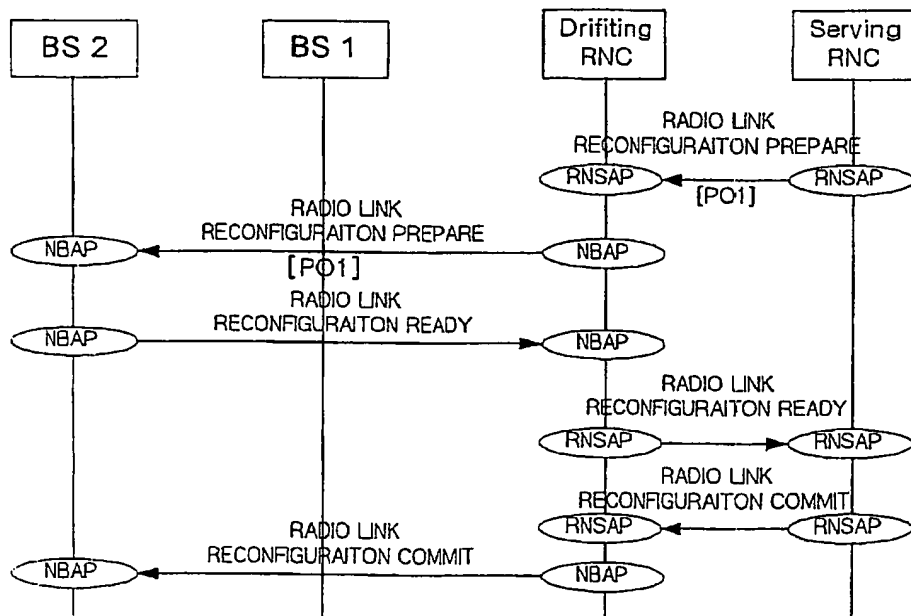


FIG.17A

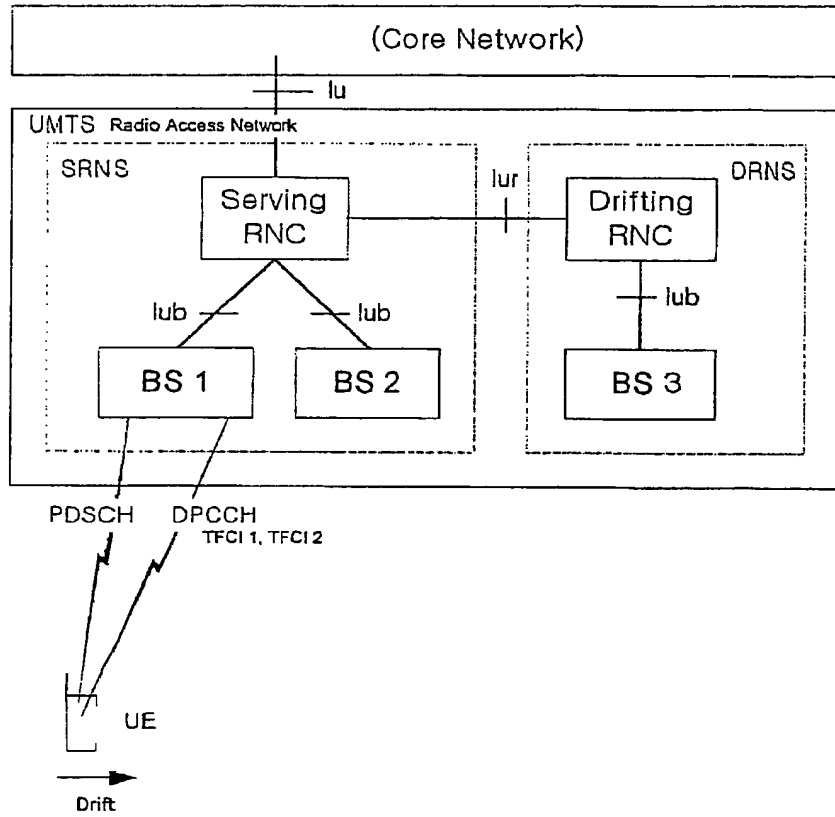


FIG.17B

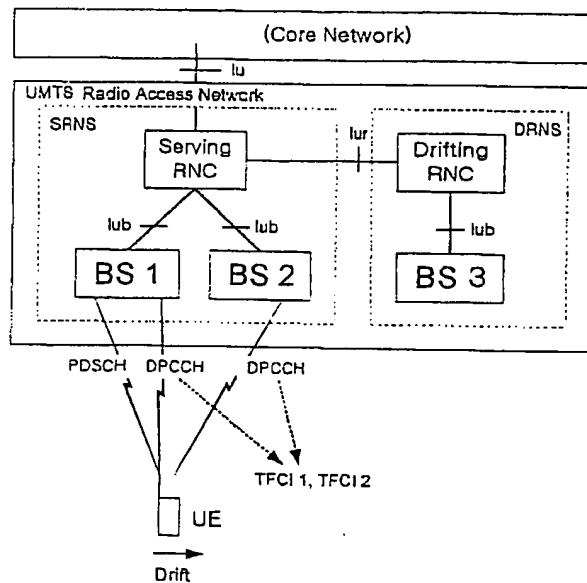


FIG.17C

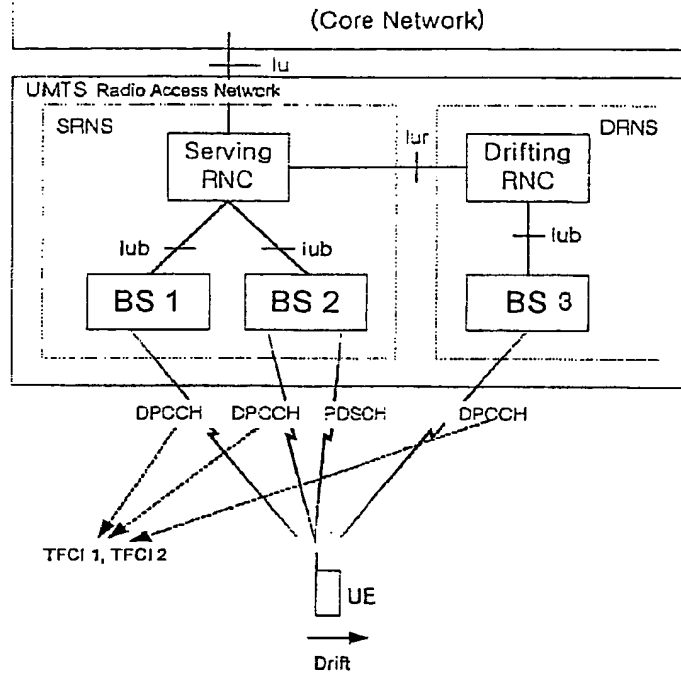


FIG.17D

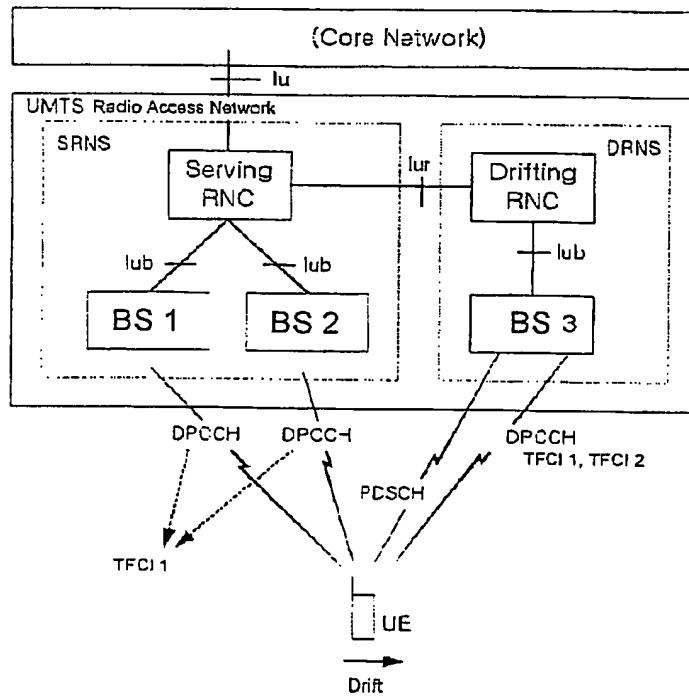
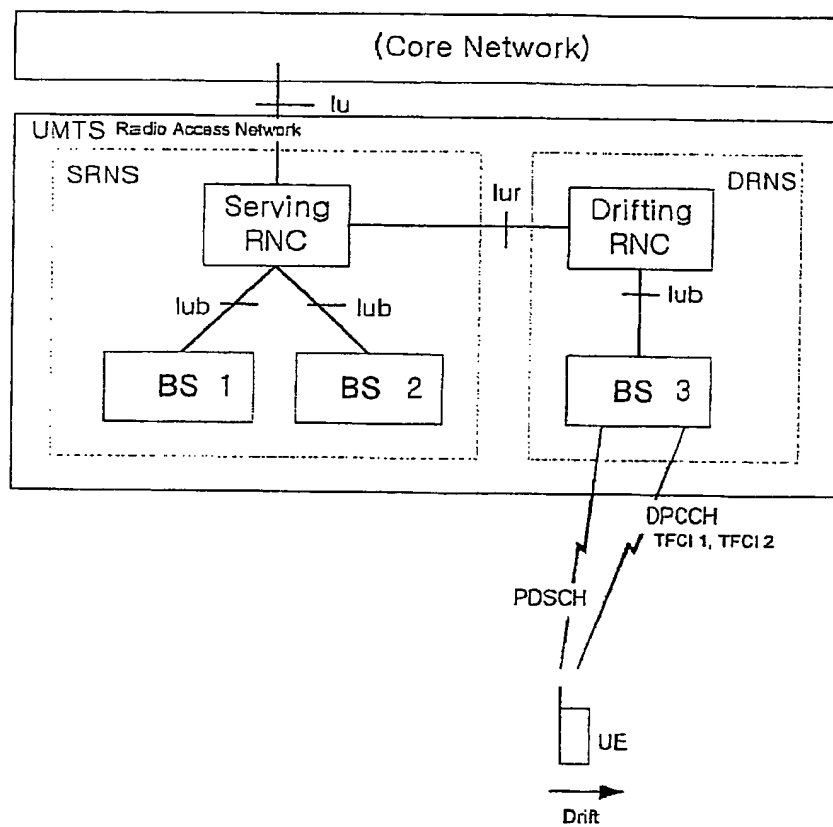


FIG.17E



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FIG.18A

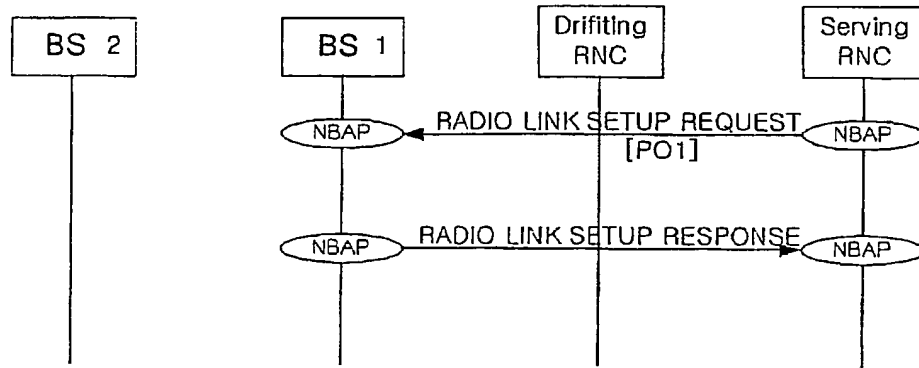


FIG.18B

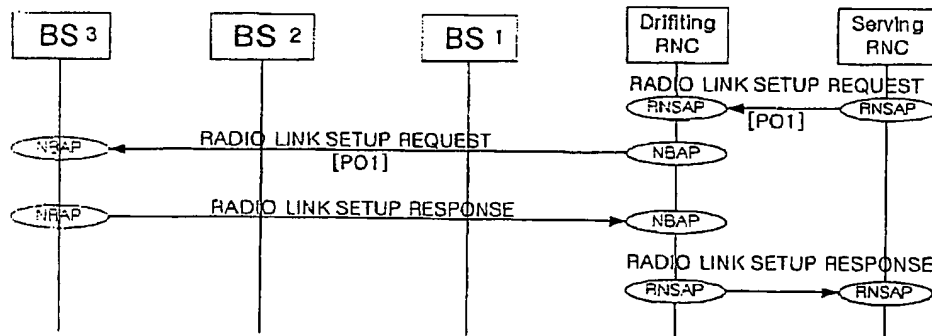
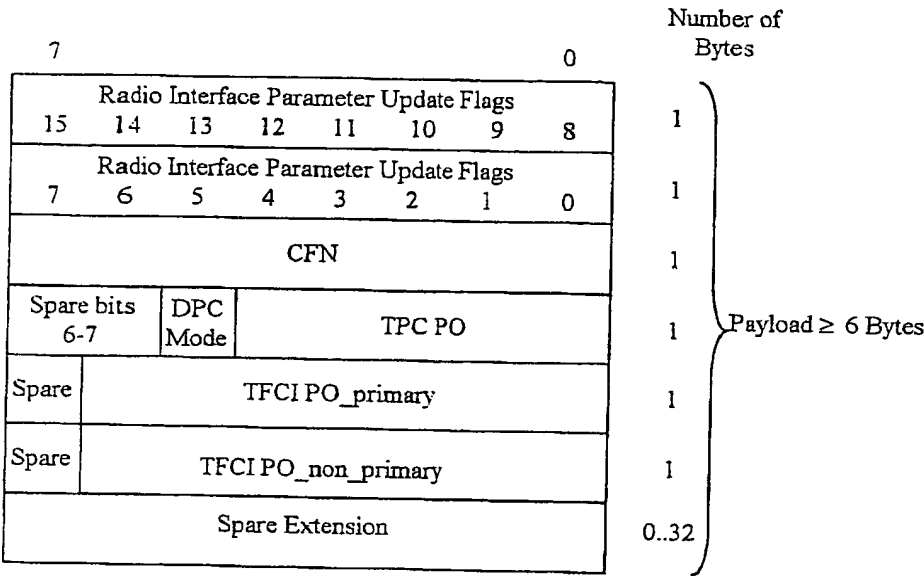


FIG.19



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FIG.20

7 0								Number of	}	Payload ≥ 3 Bytes
DSCH TFCI Power Control Flags								Bytes		
7	6	5	4	3	2	1	0	1		
Spare TFCI PO_primary								1		
Spare TFCI PO_non_primary								1		
Spare Extension								0..32		

FIG. 20

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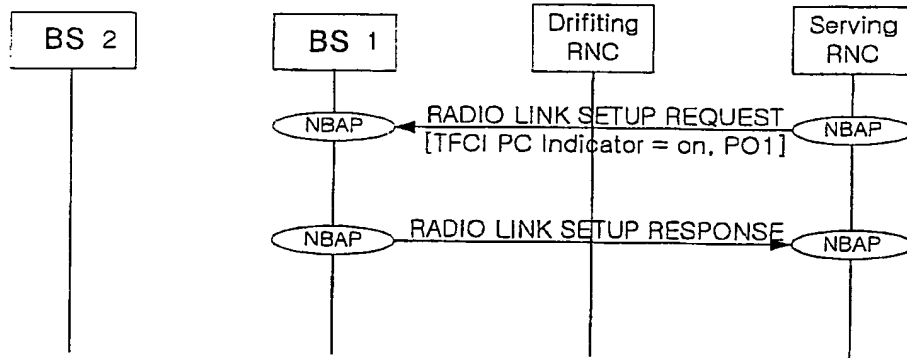


FIG. 21 B

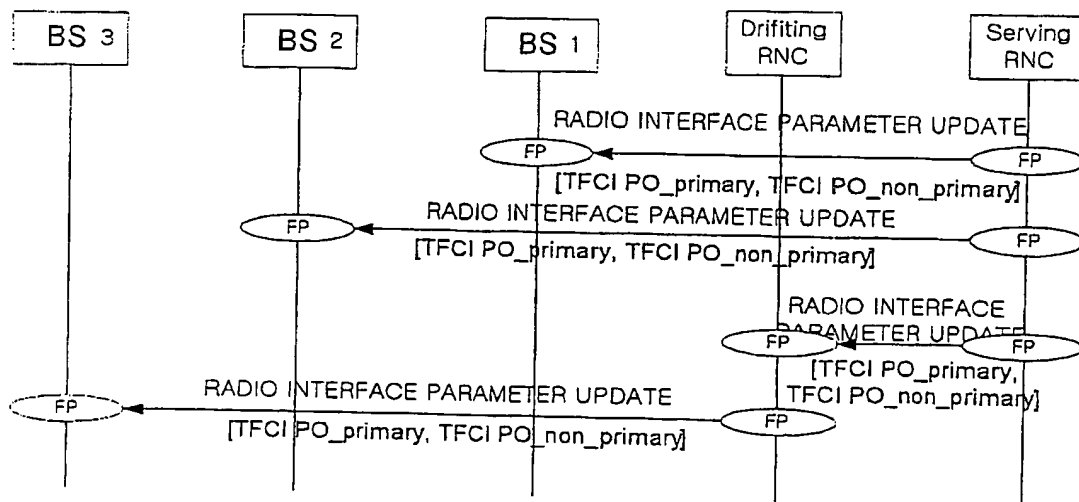


FIG.21C

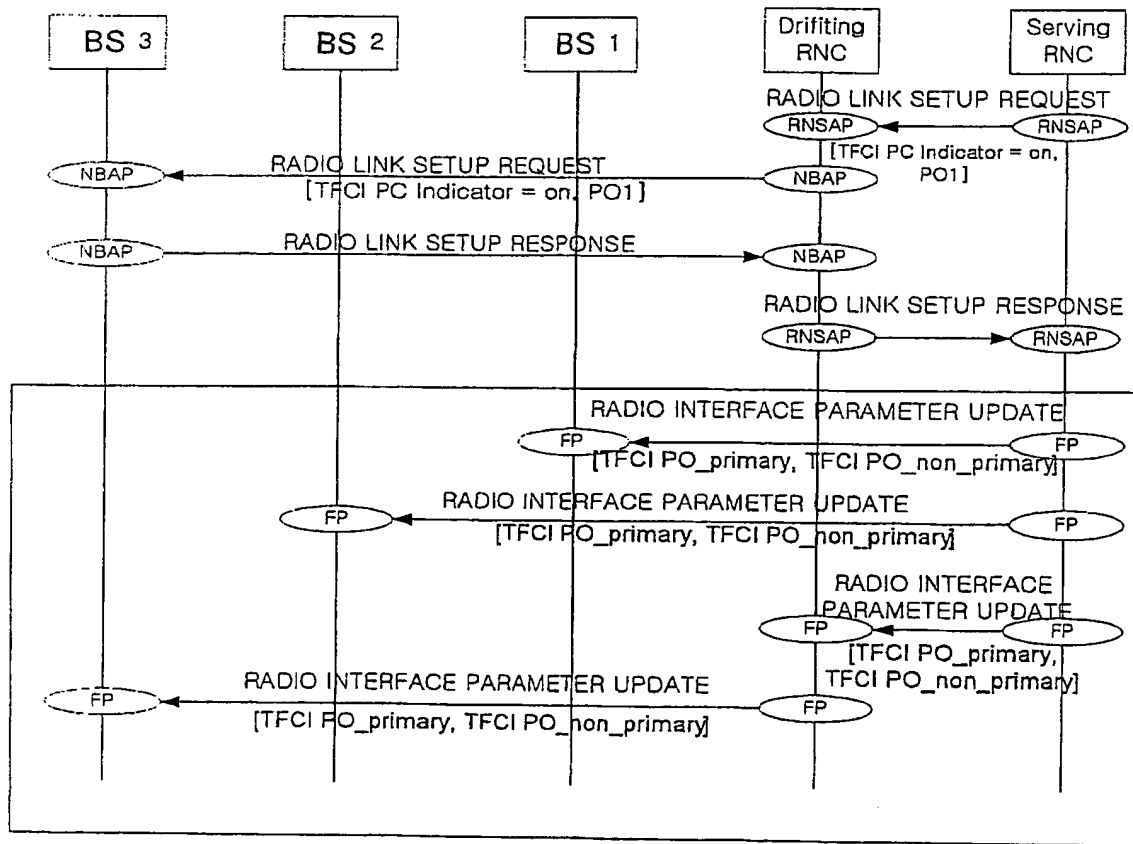


FIG.21D

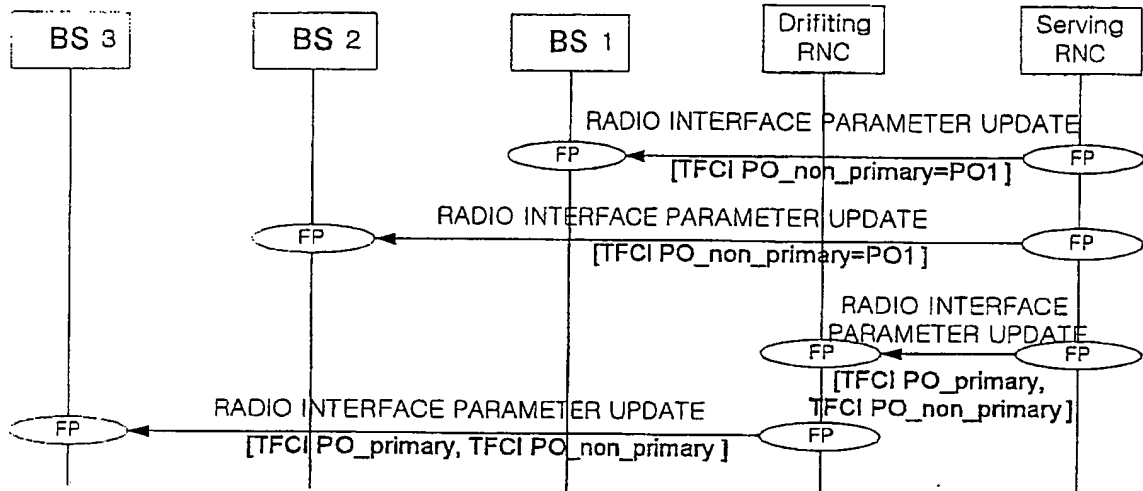


FIG.21E

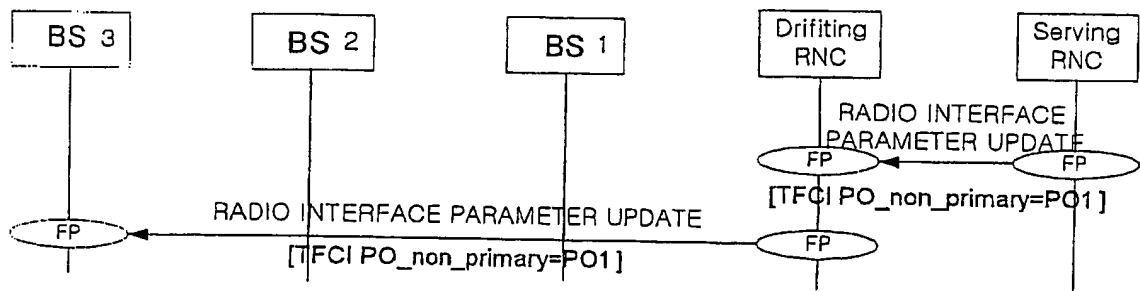


FIG.22A

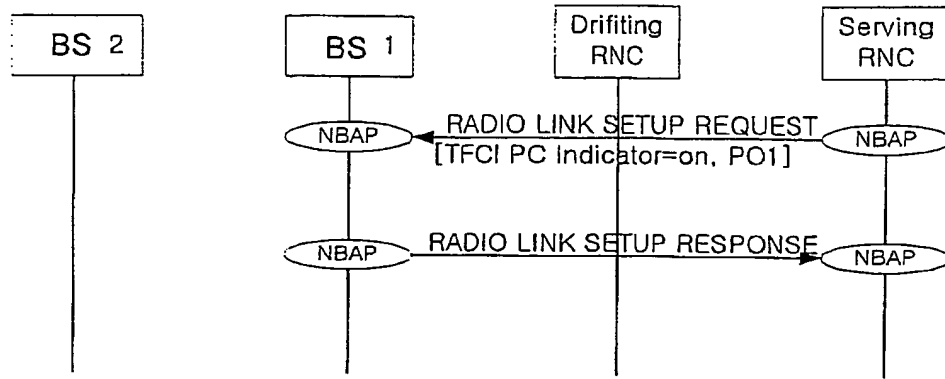


FIG.22B

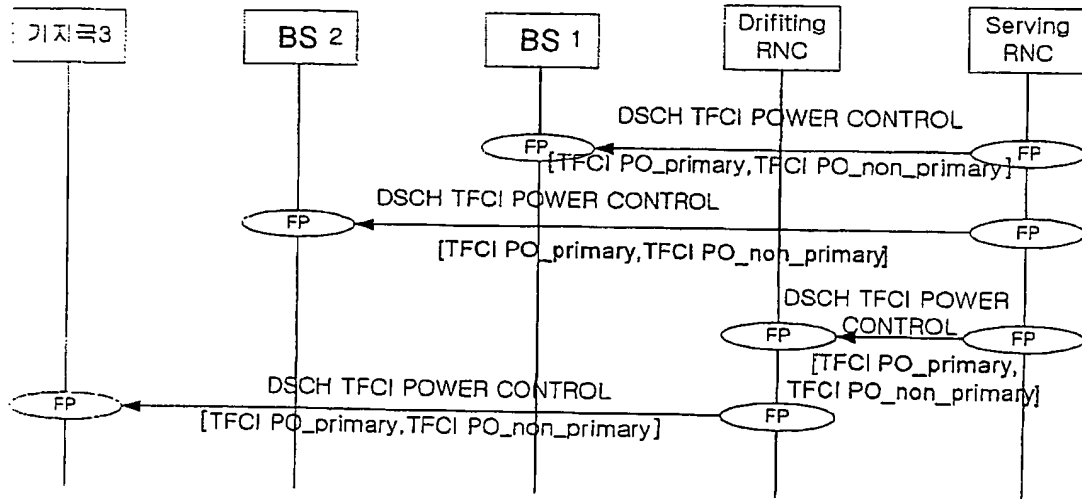


FIG.22C

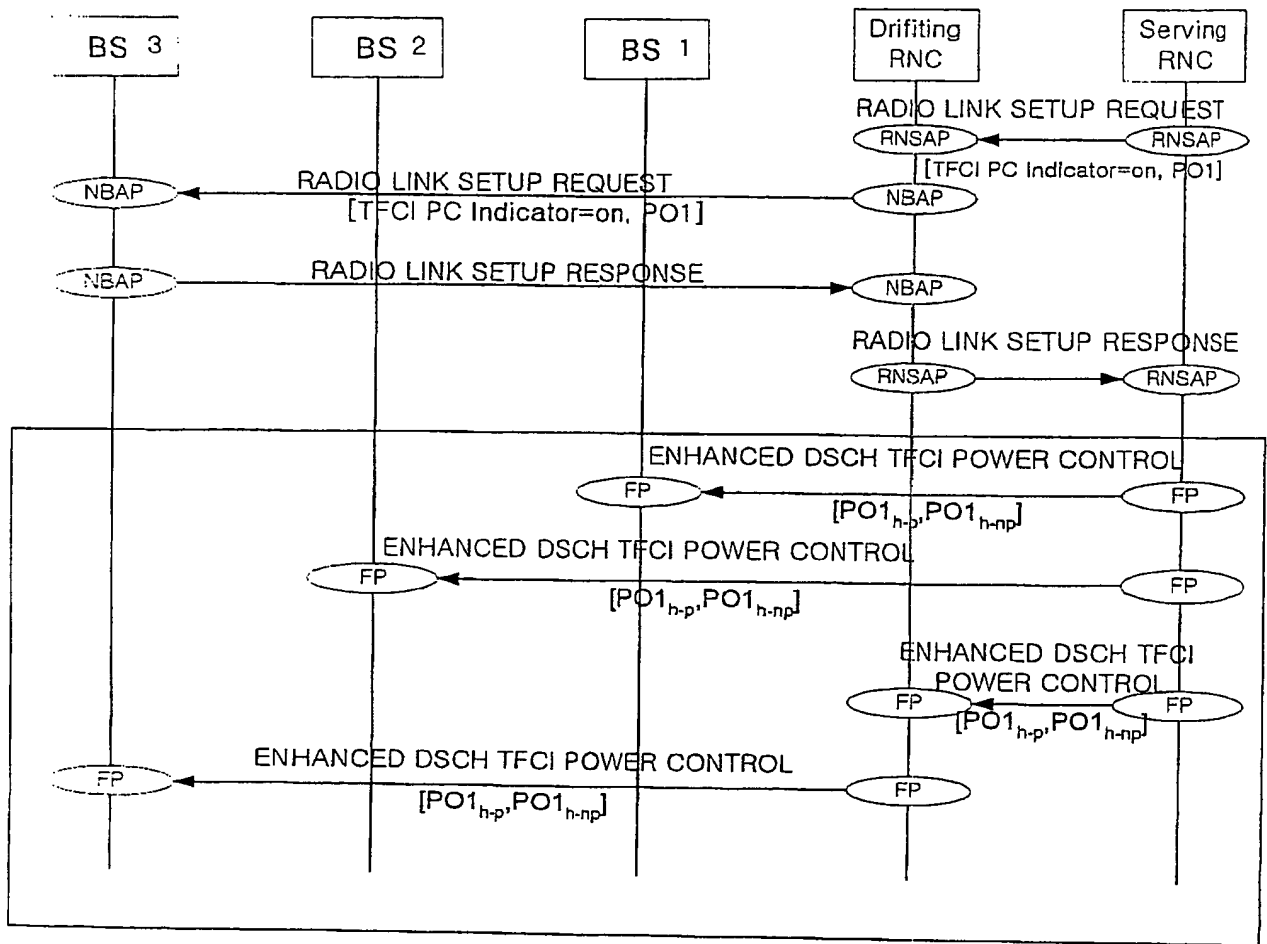


FIG.22D

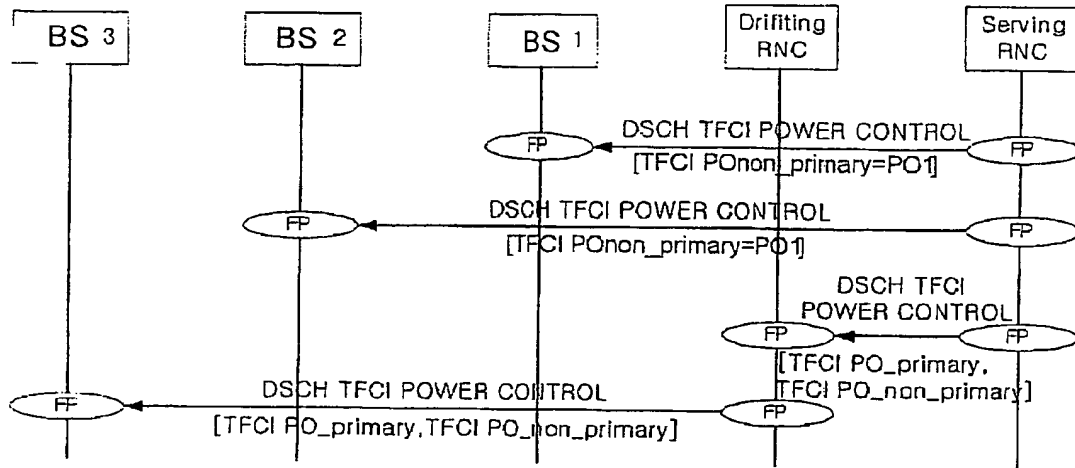


FIG.22E

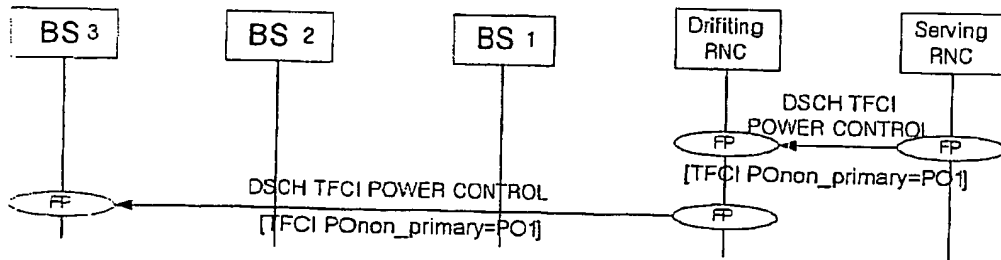


FIG.23A

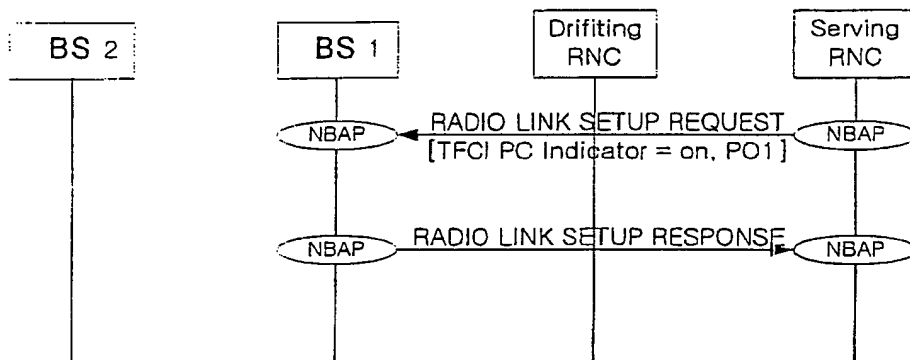


FIG.23B

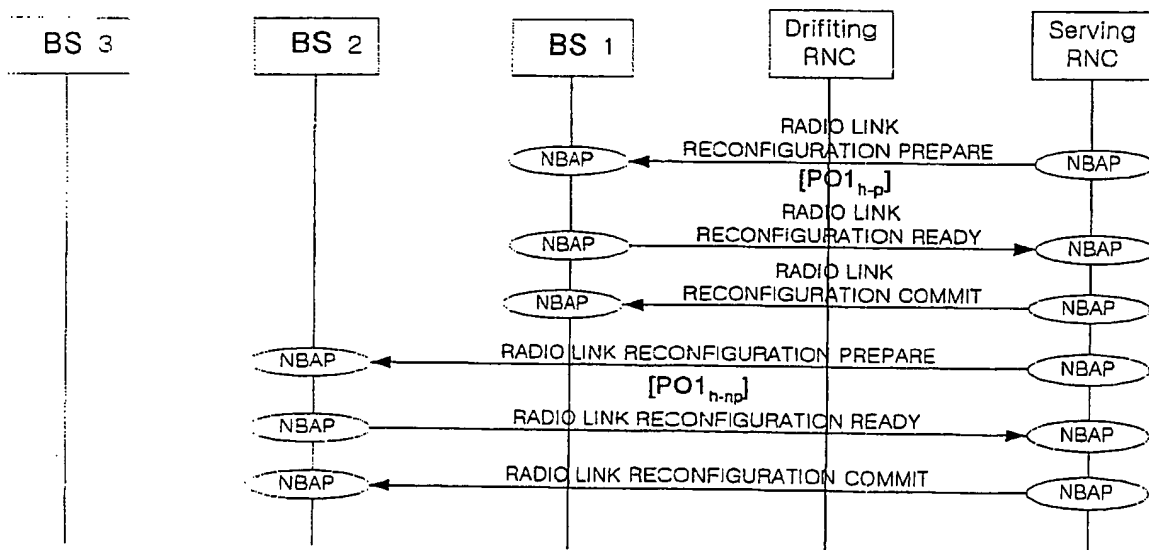


FIG.23C

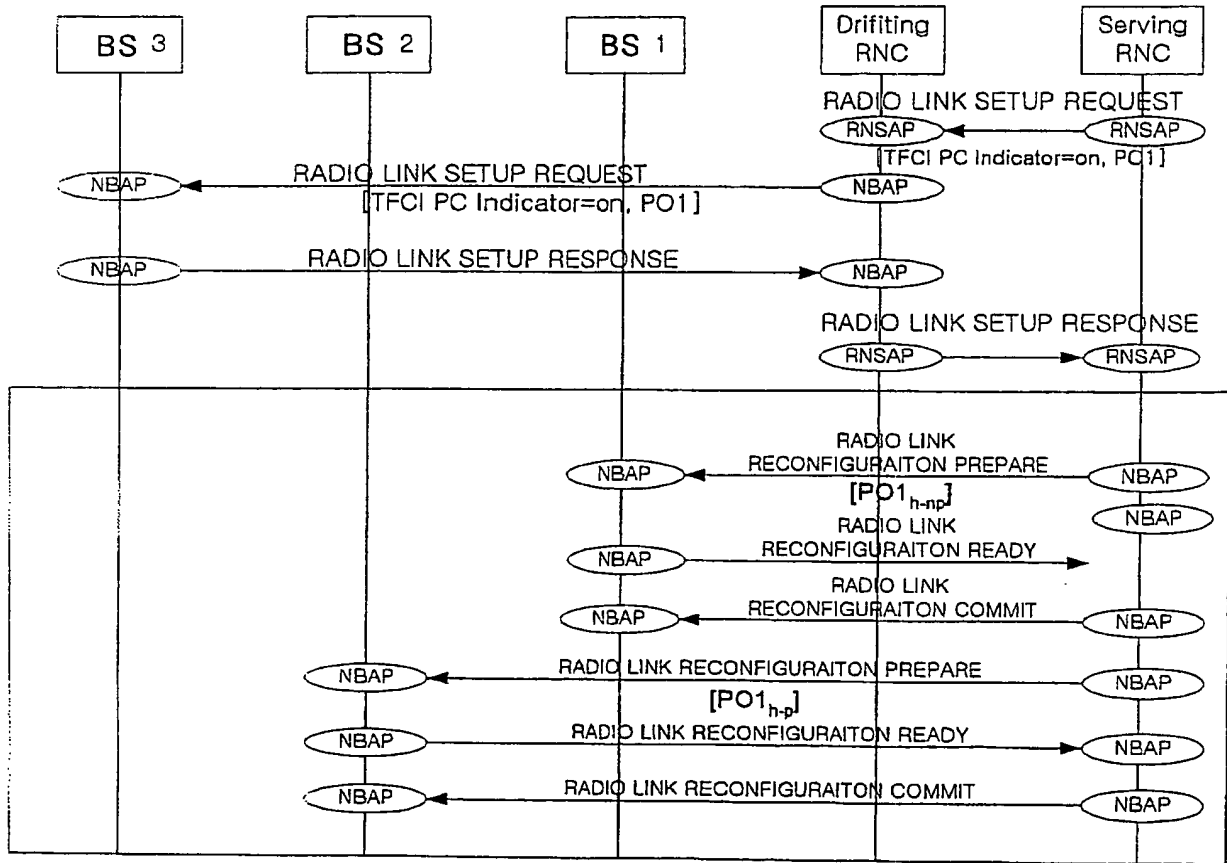


FIG. 23C

FIG.23D

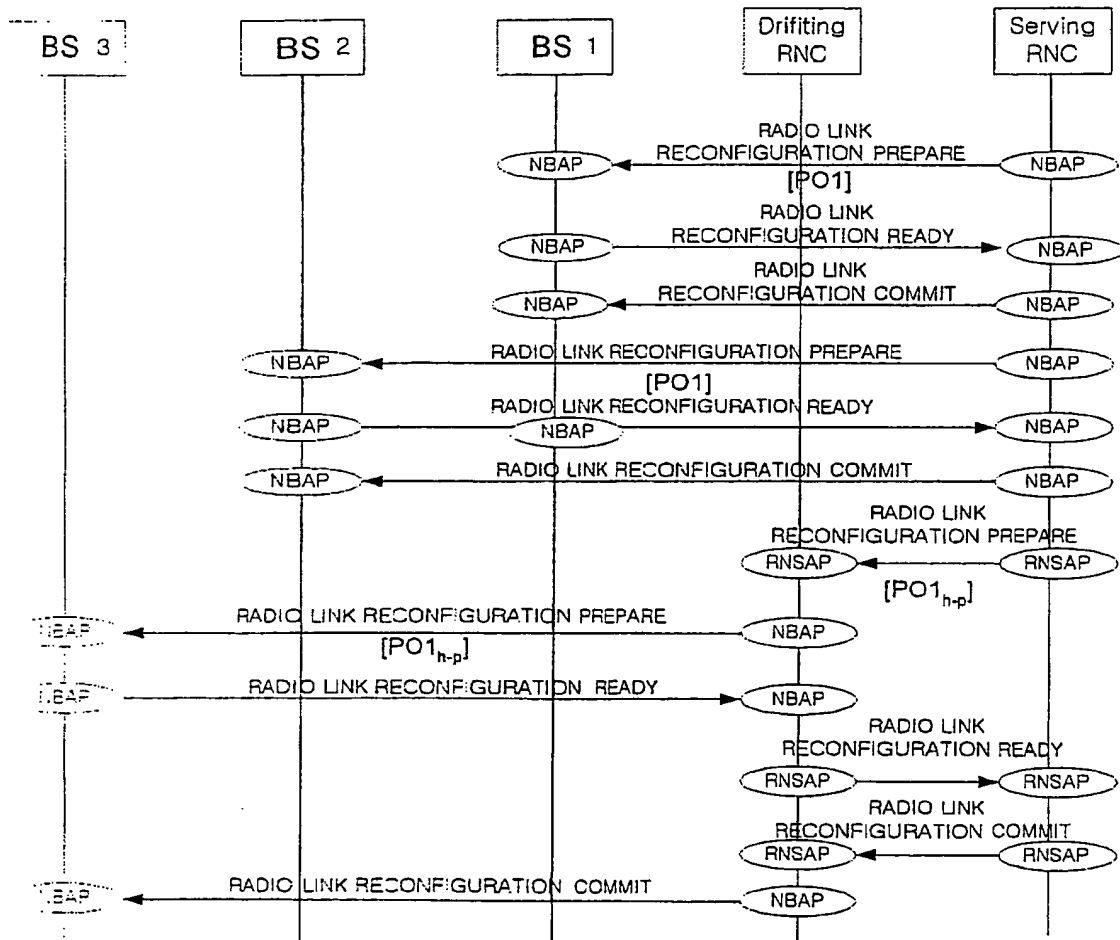


FIG. 23D

FIG.23E

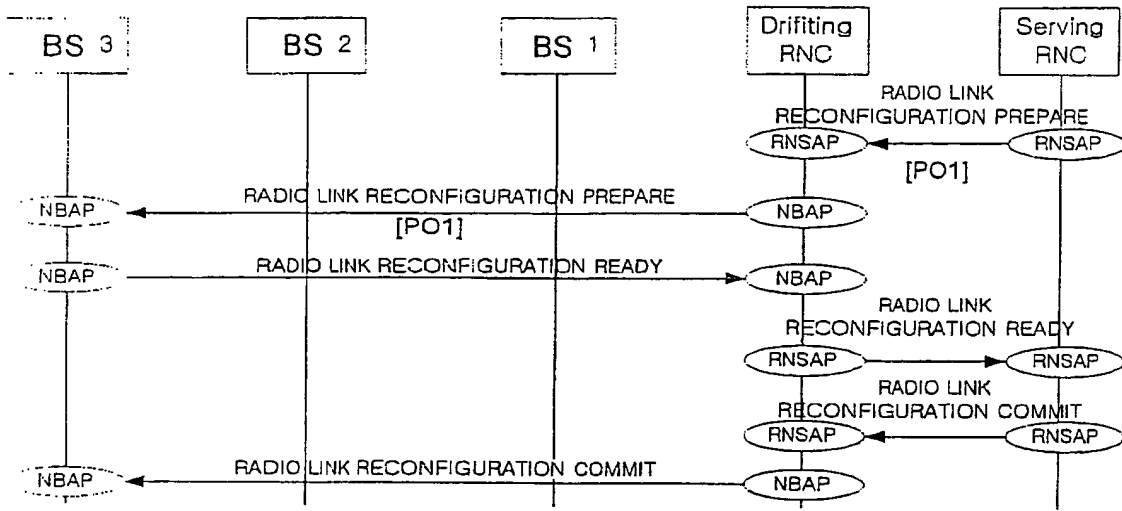


FIG.24

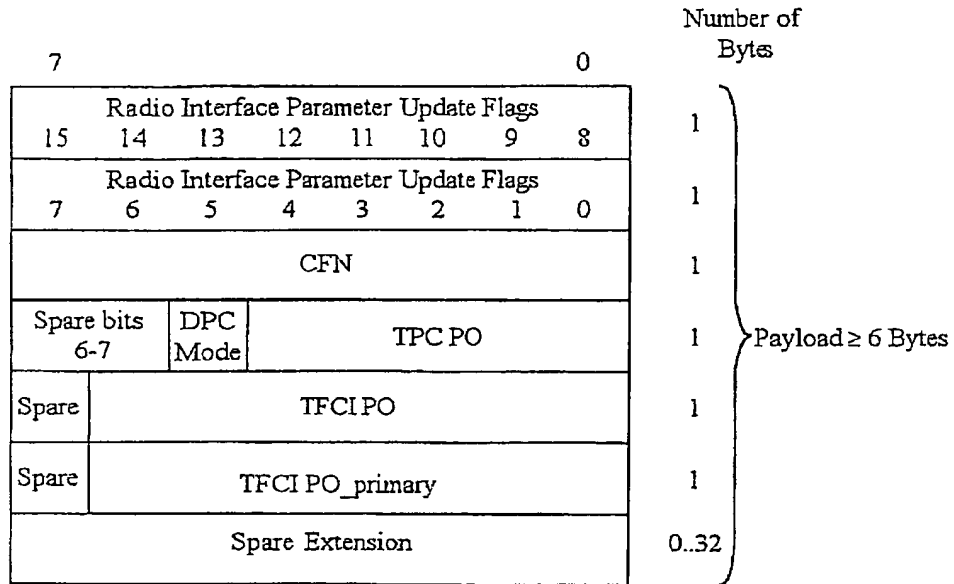


FIG.25

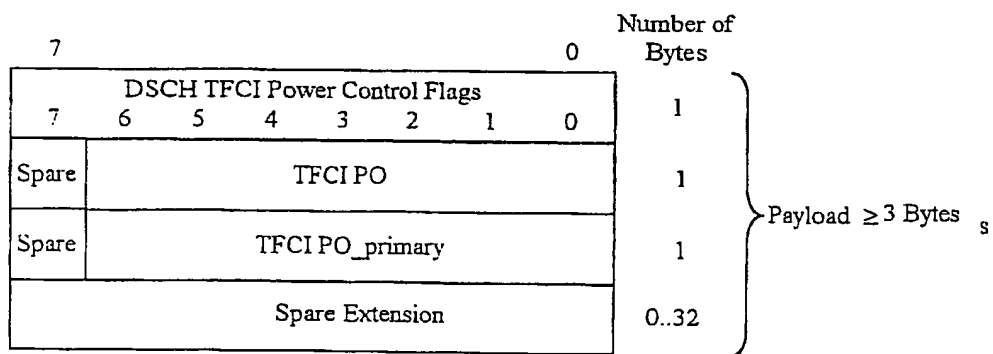


FIG.26A

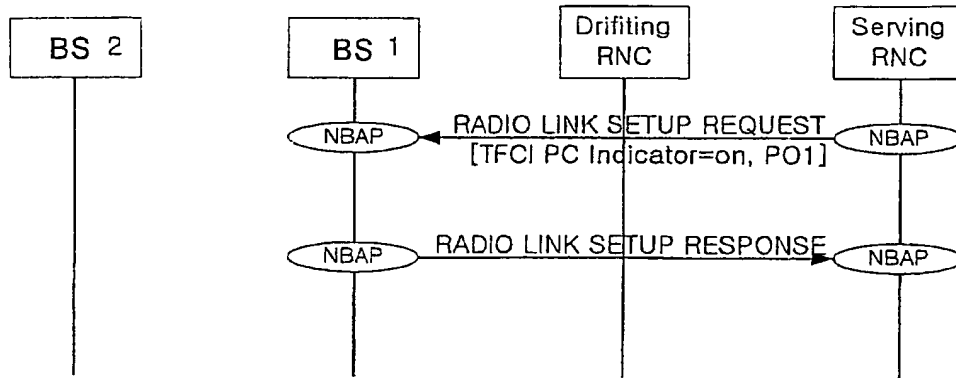


FIG.26B

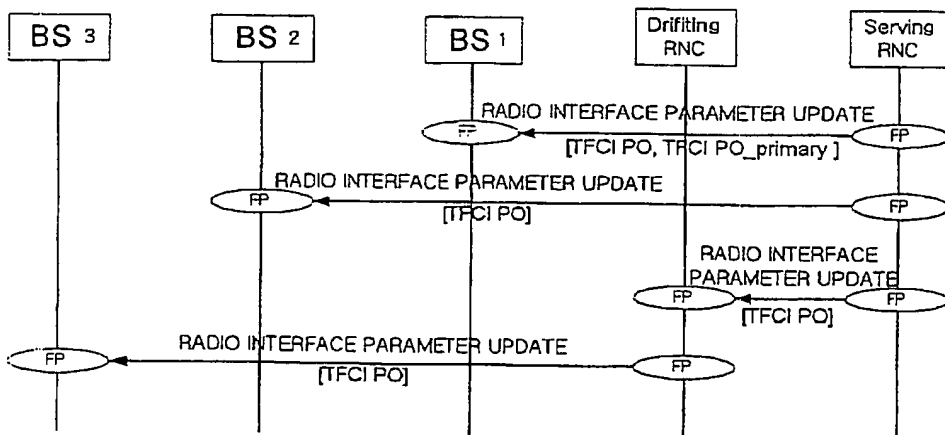


FIG.26C

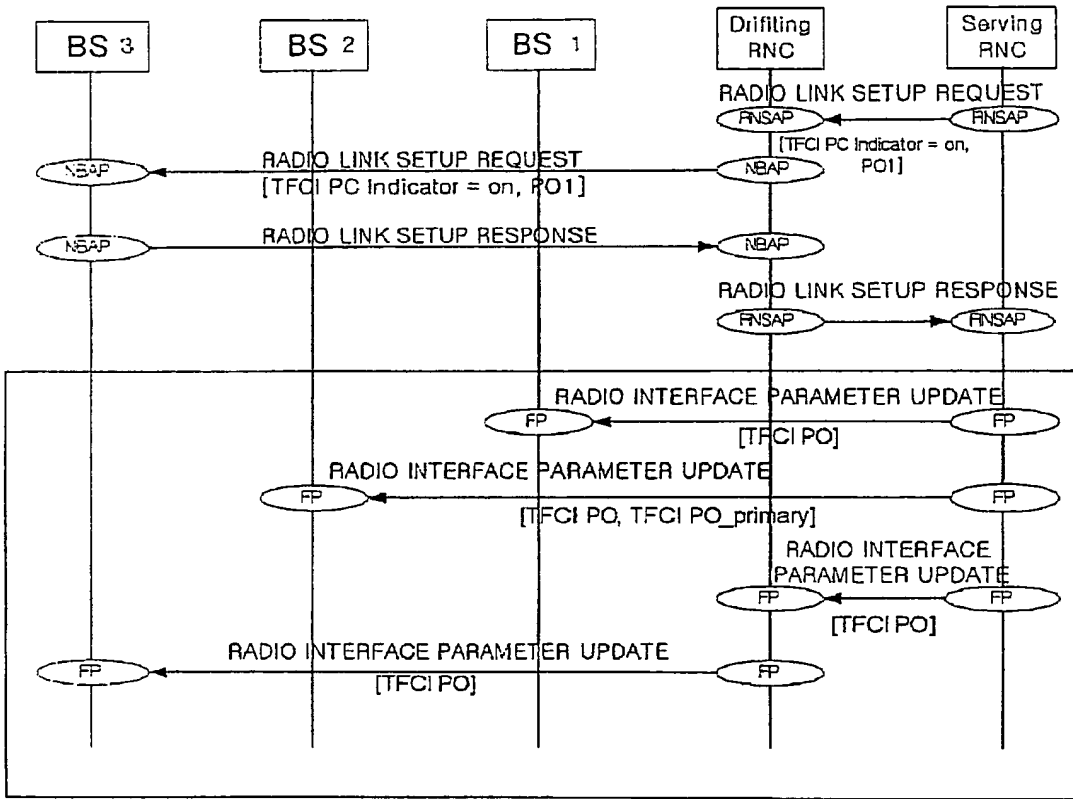


FIG. 26C

FIG.26D

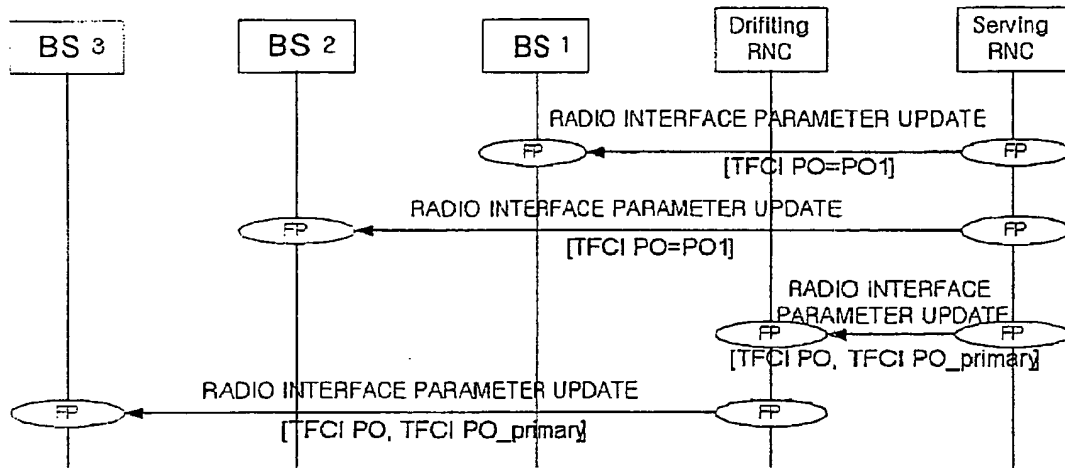


FIG.26E

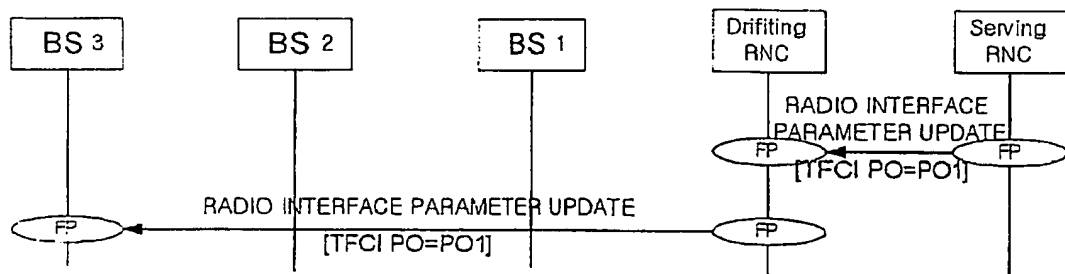


FIG.27A

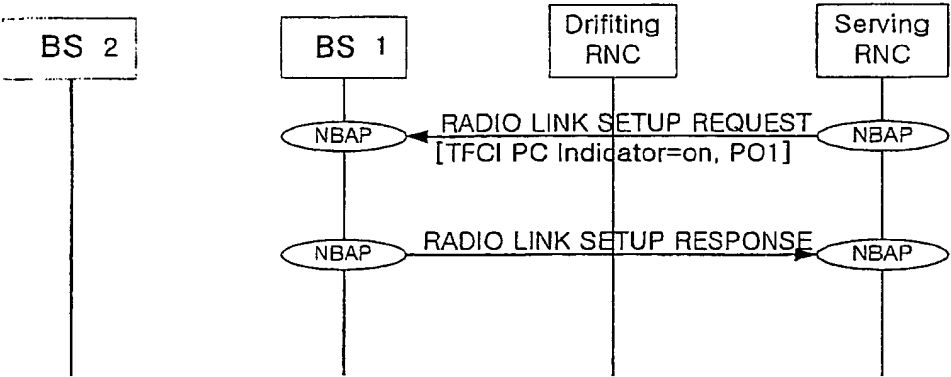


FIG.27B

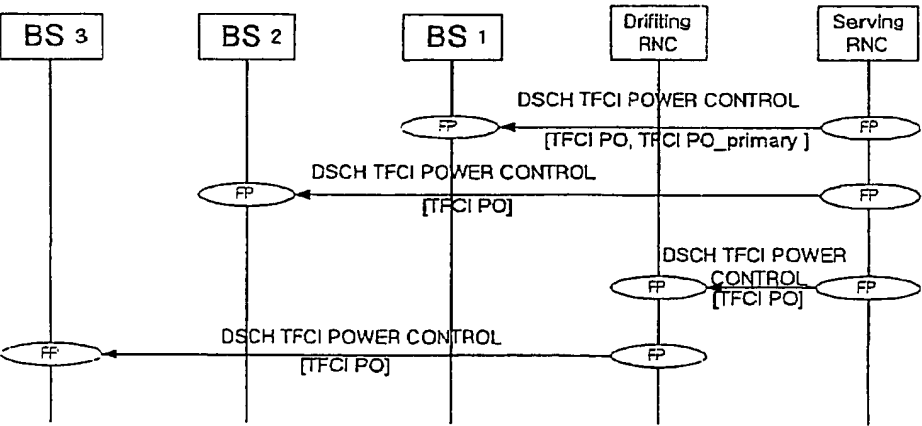
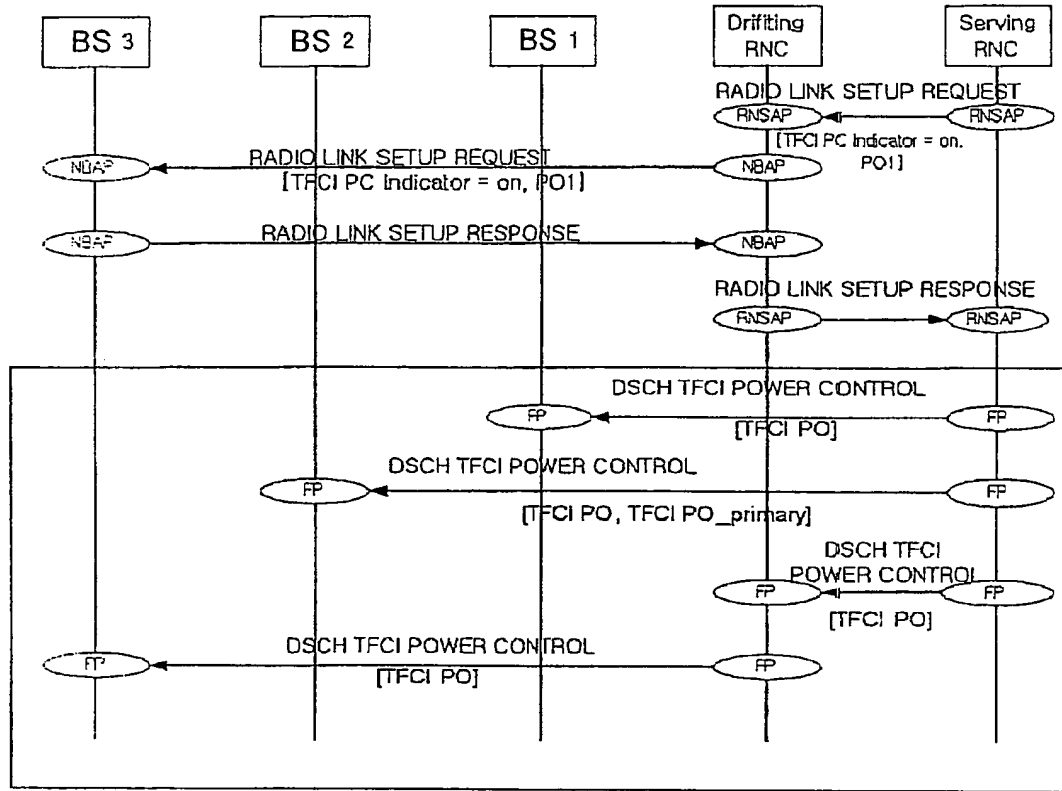


FIG.27C



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FIG.27D

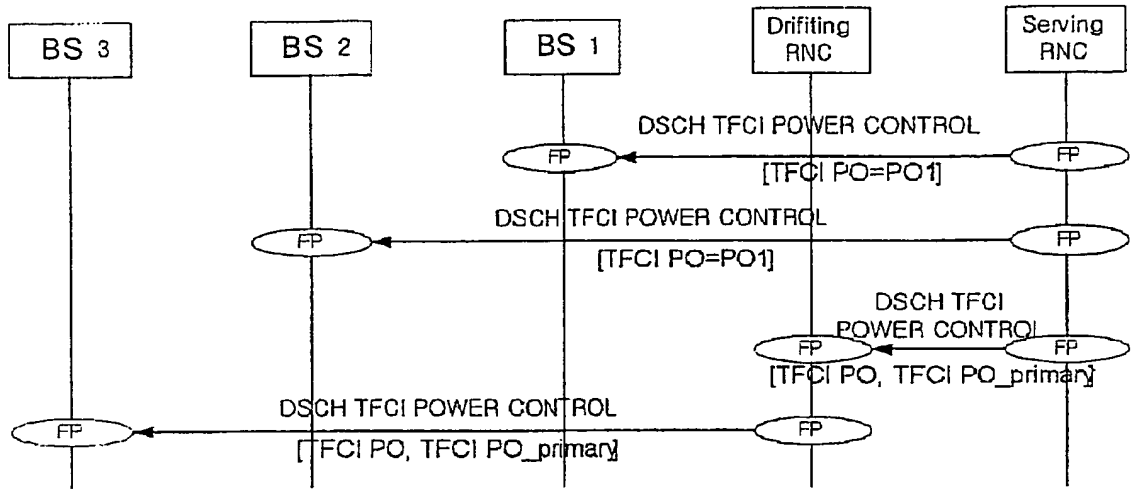


FIG.27E

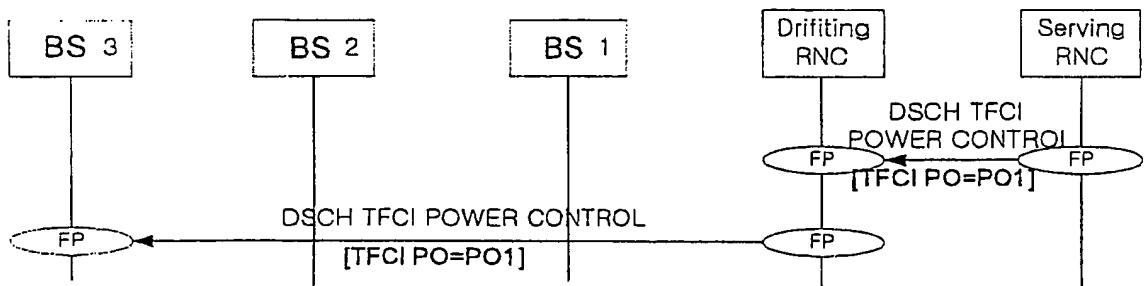


FIG.28A

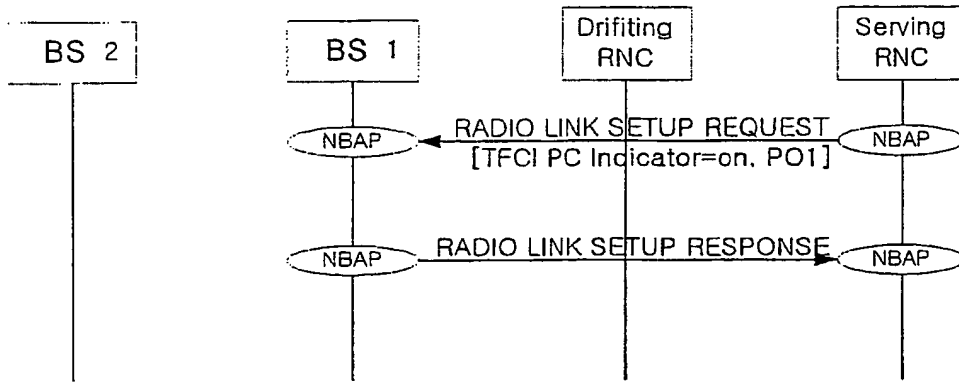


FIG.28B

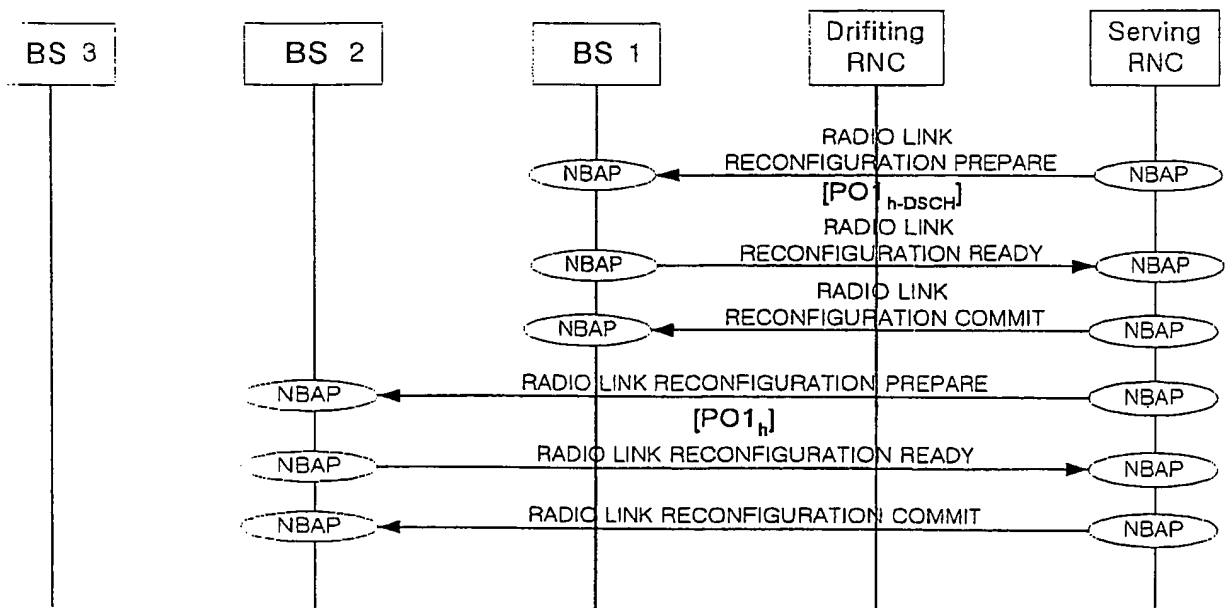
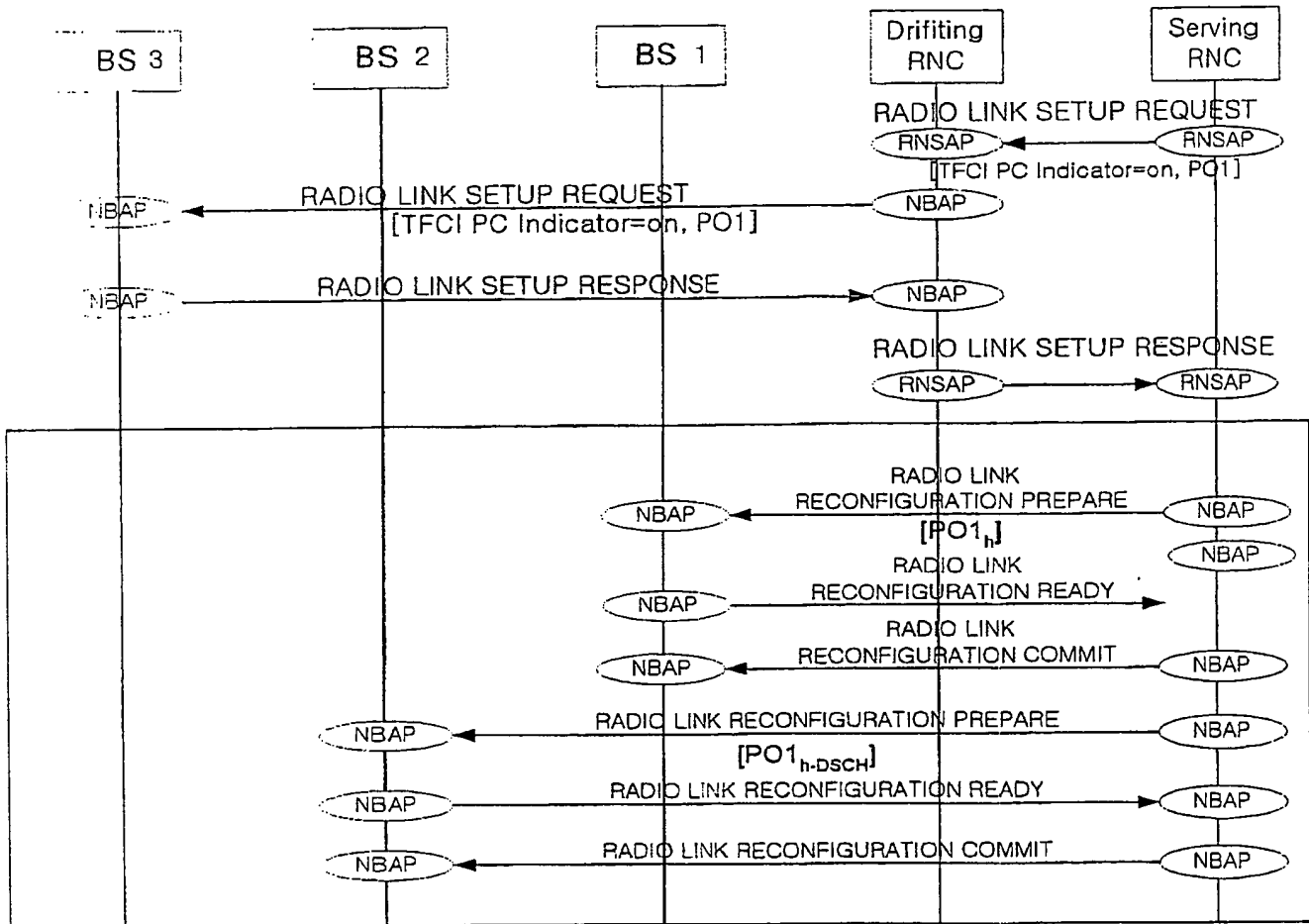


FIG.28C



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FIG.28D

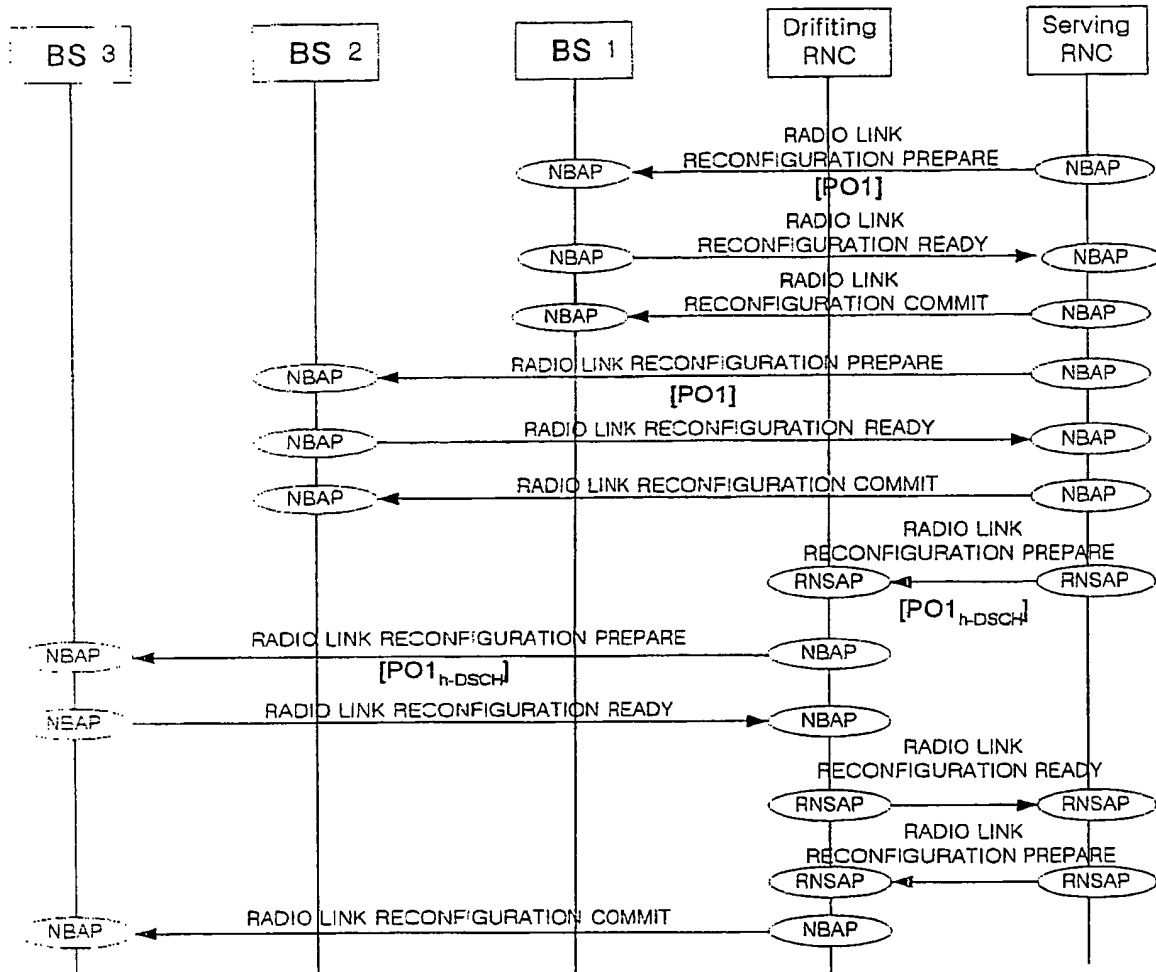
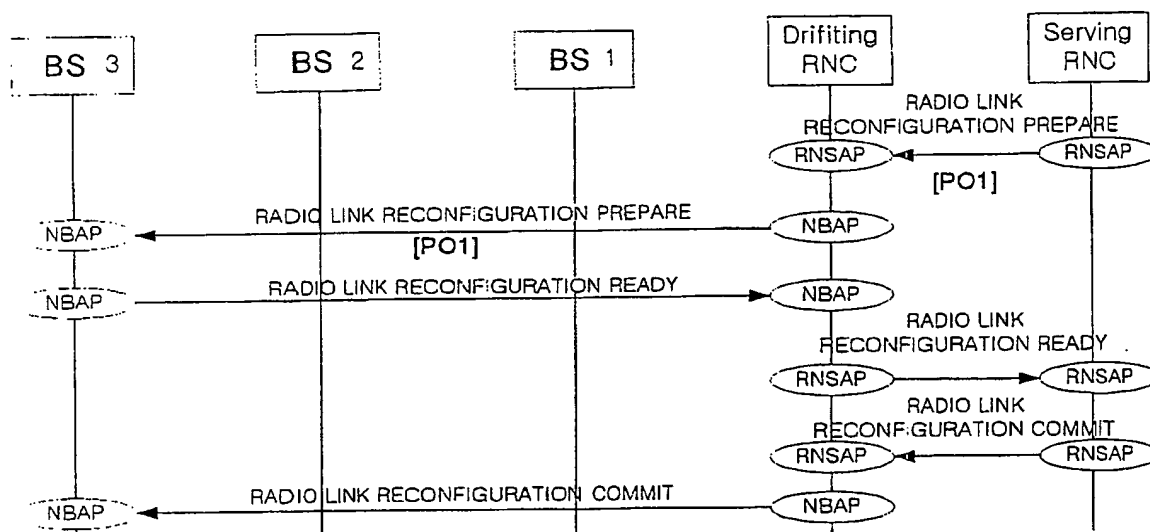


FIG.28E



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FIG.29

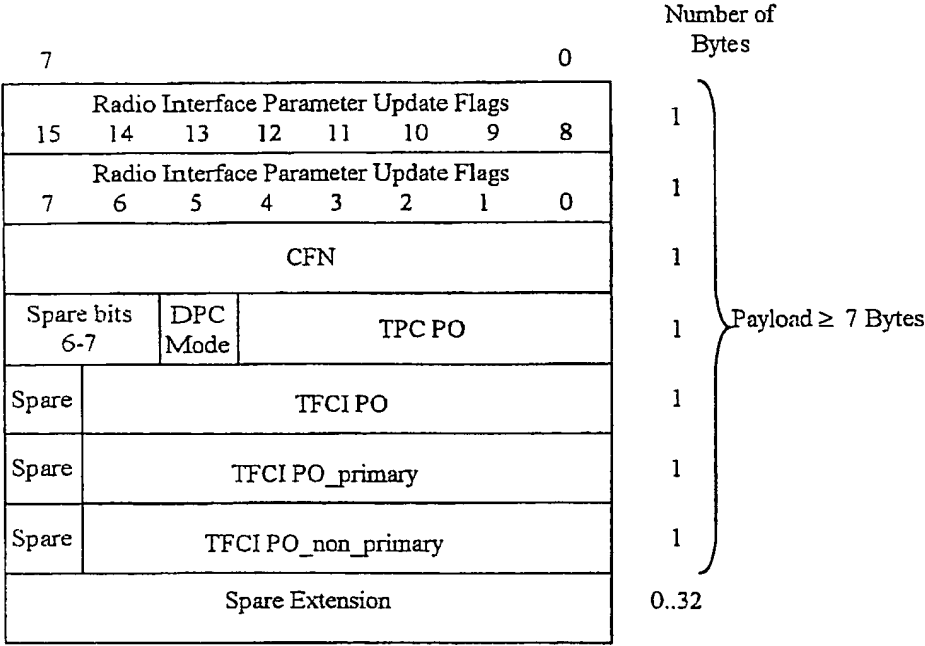


FIG.30

